APOGEE TECHNOLOGY, INC.

Application Note

Guide to Using the DDX-4100 to Implement a 5.1 Channel Audio System

Introduction

DDX® all-digital amplifiers are an excellent choice for 5.1 surround systems. The high-efficiency and power to size ratio of DDX amplifiers provide the ability to integrate power amplification inside a low-profile DVD player, A/V Receiver, or powered speaker system. When used in conjunction with a surround sound decoder IC, DDX provides a complete high quality digital surround system.

The purpose of this application note is to describe the DDX-4100 I^2C register settings necessary to implement a 5.1 channel reference design. Schematics and register settings are provided for the following two design examples.

Design 1: A 5.1 channel design with the DDX-4100's each having a unique device address (Refer to DDX-4100 errata at; http://www.apogeeddx.com/ER_DDX_4100.pdf.).

Design 2: A 5.1 channel design sharing the same device address (Two I^2C SCL's are needed for this configuration). This configuration enables additional subwoofer channel gain by using the DDX-4100 bass/treble boost settings.

The application note also includes, in the Appendices, system configuration information to meet product power output requirements, use of the bass/treble functions of the DDX-4100 and suggestions for the proper implementation of the subwoofer channel.

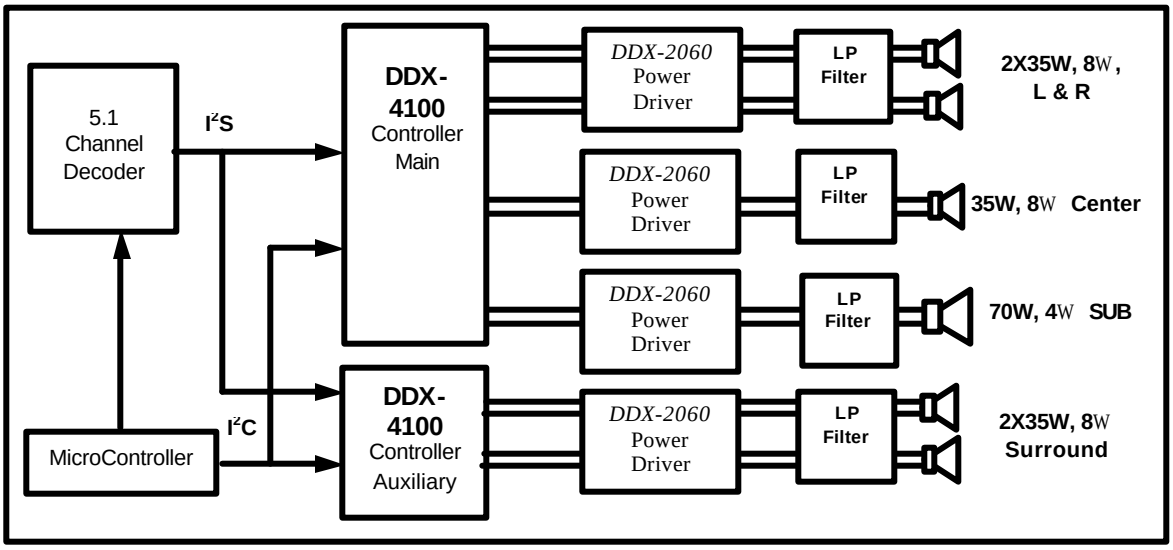
Copyright Apogee Technology, Inc 2002
(All Rights Reserved)

Design Example 1

Design a DDX 5.1 channel amplifier circuit with 5 x 35W + 1x70W, 6 channel I²S input, MCU control of I²C, and local regulation of logic power supplies. A 5.1 system with I²S inputs are assumed as well as the LFE and CENTER channels are connected to the Main Controller's Right Surround channel and Left Surround respectively. The LS and RS channels are connected to the Aux Controller's LS/RS channels.

The Main/Aux Select is done in this example by using device select addressing. By grounding the SA pin on the Main controller it's device address is 0x0011110. The Aux controller's address is 0x0011111 since it's SA pin is pulled high. In this demonstration only one SCL clock is needed from the micro-controller and the device address selects which device the micro-controller is interfacing too (an example with two SCL's is shown in design example two). When using a single SCL clock and two processors SA must be tied to VDD and SDI1 to GND on the second processor, refer to DDX-4100 errata at; http://www.apogeeddx.com/ER_DDX_4100.pdf.

BLOCK DIAGRAM for DESIGN EXAMPLE 1



I²C COMMANDS

The first I²C register settings are used to reset the main and auxiliary ICs. The digital gain is also set to the maximum level for surround sound playback (digital gain of 9dB or a factor of 3) with compression enabled.

System Reset, Set System Gain

Main/Aux Address	R/W	REG	DATA	COMMENTS
3Ch	W	00h	00h	Soft Reset, Main Controller
3Ch	W	01h	E4h	Soft Reset, Main Controller
3Eh	W	00h	00h	Soft Reset, Auxiliary Controller
3Eh	W	01h	E4h	Soft Reset, Auxiliary Controller
3Ch	W	5Bh	6Dh	Clear DDX Reset, Set DDX Gain=3X, Proprietary (1dB/step)vol. mode, Main
3Eh	W	5Bh	6Dh	Clear DDX Reset, Set DDX Gain=3X, Proprietary (1dB/step)vol. mode, Aux
3Ch	W	26h	00h	Clear EAPD, Main
3Eh	W	26h	00h	Clear EAPD, Aux

*Unmute and Set Desired Channel Volume

Main/Aux Address	R/W	REG	DATA	COMMENTS
3Ch	W	03h		Set Volume on Right Channel to Desired Setting
3Ch	W	02h		Set Volume on Left to Desired Setting and Unmute Left and Right Channels
3Ch	W	38h		Set Volume to Desired Setting and Unmute C (LS) Channel
3Ch	W	36h		Set Volume to Desired Setting and Unmute SUB (LFE) Channel
3Eh	W	37h		Set Volume to Desired Setting and Unmute Left Surround Channel
3Eh	W	38h		Set Volume to Desired Setting and Unmute Right Surround Channel

* When using the sample rate converter (SRC), **it is mandatory to apply a valid input signal to the DDX-4100 prior to unmuting**, refer to DDX-4100 errata at; http://www.apogeeddx.com/ER_DDX_4100.pdf.

LFE Redirection via Bass Management Feature

In order for the LFE channel to have a separate filter from the Center channel bass redirection can be used to redirect the LFE channel. By Default, the bass redirection factors are set to 0xC0000h. The desired scaling factors for the LFE channel redirection should be entered into the DDX-4100 device. In this example the LFE channel is completely redirected while the remaining channels are muted (refer to the I^2C commands in the following table). The biquad filters should be written when the devices are muted, i.e., prior to the Unmute commands above.

Main/Aux Address	R/W	REG	DATA	COMMENTS
3Ch	W	73h	01h	Enable Bass-Management in Main Controller
3Ch	W	78h	00h	Write L SCALE bit [15..8] for L Channel redirection factor on Main Controller (MUTE)
3Ch	W	79h	00h	Write L SCALE bit [7..0] for L Channel redirection factor on Main Controller (MUTE)
3Ch	W	7Ah	7Fh	Write L SCALE address for L Channel redirection factor on Main Controller (MUTE)
3Ch	W	7Bh	00h	Write L SCALE bit [19..16] for L Channel redirection factor on Main Controller (MUTE)
3Ch	W	78h	00h	Write R SCALE bit [15..8] for R Channel redirection factor on Main Controller (MUTE)
3Ch	W	79h	00h	Write R SCALE bit [7..0] for R Channel redirection factor on Main Controller (MUTE)
3Ch	W	7Ah	80h	Write R SCALE address for R Channel redirection factor on Main Controller (MUTE)
3Ch	W	7Bh	00h	Write R SCALE bit [19..16] for R Channel redirection factor on Main Controller (MUTE)
3Ch	W	78h	00h	Write C (LS) SCALE bit [15..8] for C Chan redirection factor on Main Controller(MUTE)
3Ch	W	79h	00h	Write C (LS) SCALE bit [7..0] for C Chan redirection factor on Main Controller (MUTE)
3Ch	W	7Ah	81h	Write C (LS) SCALE address for C Chan redirection factor on Main Controller (MUTE)
3Ch	W	7Bh	00h	Write C(LS) SCALE bit[19..16] for C Chan redirection factor on MainController (MUTE)
3Ch	W	78h	00h	Write LFE (RS) SCALE bit [15..8]for SUB Chan redirection factor on Main Controller
3Ch	W	79h	00h	Write LFE (RS) SCALE bit [7..0] for SUB Chan redirection factor on Main Controller
3Ch	W	7Ah	82h	Write LFE (RS) SCALE address for SUB Chan redirection factor on Main Controller
3Ch	W	7Bh	08h	Write LFE (RS) SCALE bit [19..16] for SUB Chan redirection factor on Main Controller
3Ch	W	78h	00h	Write C SCALE bit [15..8] for C Chan redirection factor on Main Controller (MUTE)
3Ch	W	79h	00h	Write C SCALE bit [7..0] for C Chan redirection factor on Main Controller (MUTE)
3Ch	W	7Ah	83h	Write C SCALE address for C Chan redirection factor on Main Controller (MUTE)
3Ch	W	7Bh	00h	Write C SCALE bit [19..16] for C Chan redirection factor on Main Controller (MUTE)
3Ch	W	78h	00h	Write LFE SCALE bit [15..8]for LFE Chan redirection factor on Main Controller (MUTE)
3Ch	W	79h	00h	Write LFE SCALE bit [7..0] for LFE Chan redirection factor on Main Controller (MUTE)
3Ch	W	7Ah	84h	Write LFE SCALE address for LFE Chan redirection factor on Main Controller (MUTE)
3Ch	W	7Bh	00h	Write LFE SCALE bit [19..16] for LFE Ch redirection factor on Main Controller (MUTE)

BIQUAD Coefficients (Optional)

As an additional example of I^2C setting, biquad filters are used to perform speaker equalization and crossover functions. The biquad filters should be written when the devices are muted, i.e., prior to the Unmute commands above.

The biquad coefficients were obtained using Apogee's Filter generation software and were generated in order to equalize a +2dB bump at 1kHz with Q = 1.414 on the L/R/LS/RS/C channels. On the LFE channel a 2nd order Butterworth Low-pass filter with a cutoff of 225Hz was used.

L/R/LS/RS/C Coefficients:

B2: 0x73633h
(B0)-1: 0 xFE8DF h
A2: 0x71F1Fh
A1/2: 0x88107h
B1/2: 0x88107h

SUB Coefficients:

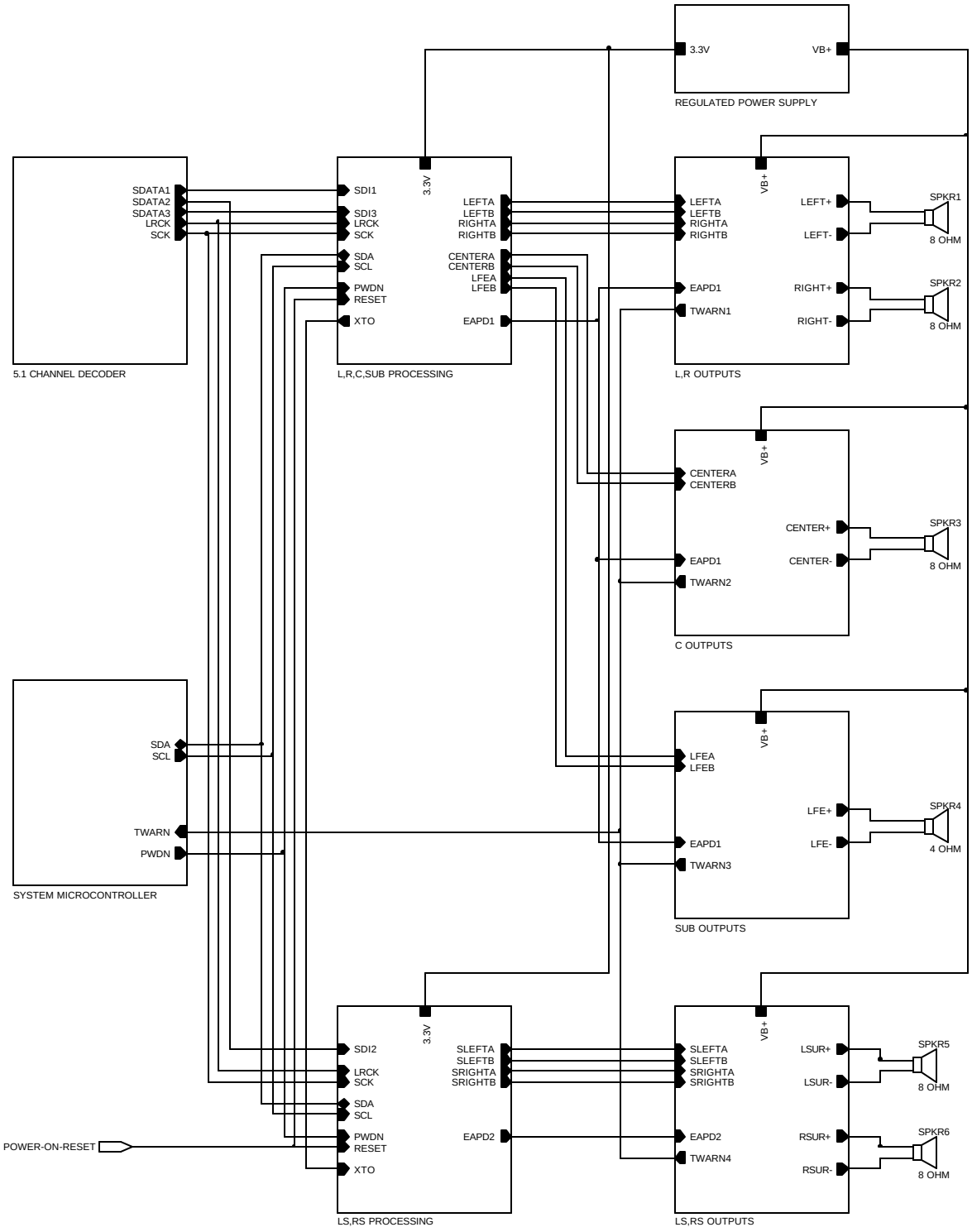
B2: 0x0006Fh
(B0)-1: 0x80070h
A2: 0x7AC6Fh
A1/2: 0x82AA7Fh
B1/2: 0x0006Fh

Following are the steps necessary to write coefficients via I^2C

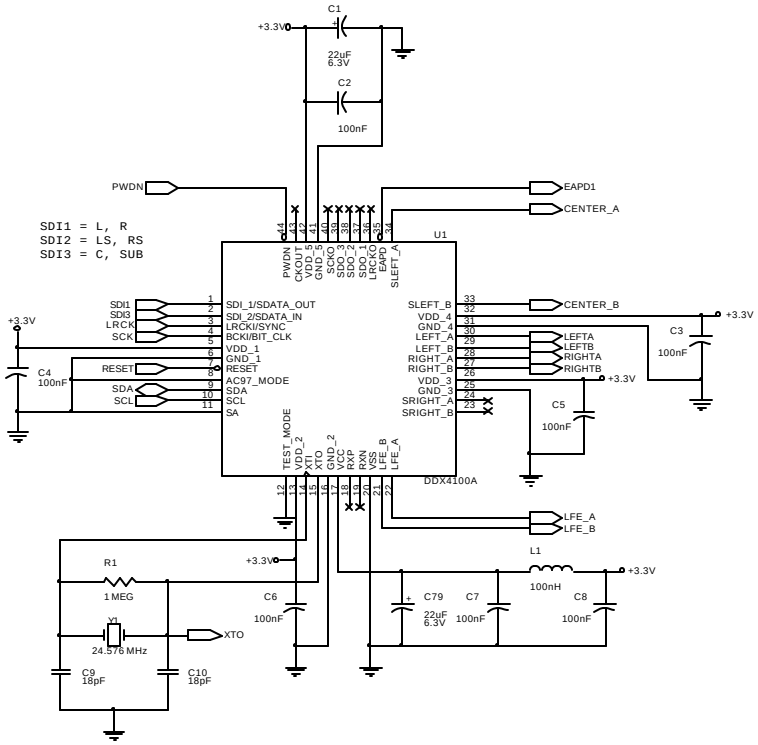
Write 8 middle data bits at I^2C address 78h
Write 8 lower data bits at I^2C address 79h
Write 8 bit address at I^2C address 7Ah coeff INDEX +40h
Write 4 upper data bits and R/W bit at I^2C address

Main/Aux Address	R/W	REG	DATA	COMMENTS
3Ch	W	78h	36h	Write [B2 Biqaud 0] Coeff bit [15..8] for LR Channel on Main Controller
3Ch	W	79h	33h	Write [B2 Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
3Ch	W	7Ah	40h	Write [B2 Biquad 0] Coeff address for LR Channel on Main Controller
3Ch	W	7Bh	07h	Write [B2 Biquad 0] Coeff bit [19..16] for LR Channel on Main Controller
3Ch	W	78h	E8h	Write [((B0) –1) Biquad 0] Coeff bit [15..8] for LR Channel on Main Controller
3Ch	W	79h	DFh	Write [((B0) –1) Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
3Ch	W	7Ah	41h	Write [((B0) –1) Biquad 0] Coeff address for LR Channel on Main Controller
3Ch	W	7Bh	0Fh	Write [((B0) –1) Biquad 0] Coeff bit [19..16] for LR Channel on Main Controller
3Ch	W	78h	1Fh	Write [A2 Biqaud 0] Coeff bit [15..8] for LR Channel on Main Controller
3Ch	W	79h	1Fh	Write [A2 Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
3Ch	W	7Ah	42h	Write [A2 Biquad 0] Coeff address for LR Channel on Main Controller
3Ch	W	7Bh	07h	Write [A2 Biquad 0] Coeff bit [19..16] for LR Channel on Main Controller
3Ch	W	78h	81h	Write [(A1/2) Biquad 0] Coeff bit [15..8] for LR Channel on Main Controller
3Ch	W	79h	07h	Write [(A1/2) Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
3Ch	W	7Ah	43h	Write [(A1/2) –1) Biquad 0] Coeff address for LR Channel on Main Controller
3Ch	W	7Bh	08h	Write [(A1/2) –1) Biquad 0] Coeff bit [19..16] for LR Channel on Main Controller
3Ch	W	78h	81h	Write [(B1/2) Biquad 0] Coeff bit [15..8] for LR Channel on Main Controller
3Ch	W	79h	07h	Write [(B1/2) Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
3Ch	W	7Ah	44h	Write [(B1/2) –1) Biquad 0] Coeff address for LR Channel on Main Controller
3Ch	W	7Bh	08h	Write [(B1/2) –1) Biquad 0] Coeff bit [19..16] for LR Channel on Main Controller
3Ch	W	78h	36h	Write [B2 Biqaud 0] Coeff bit [15..8] for C (LSRS) Channel on Main Controller

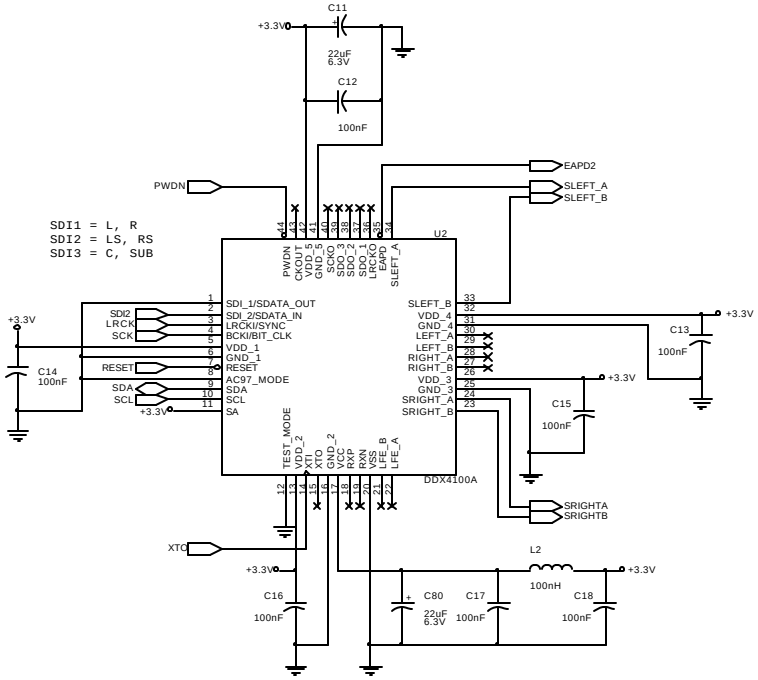
3Ch	W	79h	33h	Write [B2 Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on Main Controller
3Ch	W	7Ah	45h	Write [B2 Biquad 0] Coeff address for C (LSRS) Channel on Main Controller
3Ch	W	7Bh	07h	Write [B2 Biquad 0] Coeff bit [19..16] for C (LSRS) Channel on Main Controller
3Ch	W	78h	E8h	Write [((B0) –1) Biquad 0] Coeff bit [15..8] for C (LSRS) Channel on Main Controller
3Ch	W	79h	DFh	Write [((B0) –1) Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on Main Controller
3Ch	W	7Ah	46h	Write [((B0) –1) Biquad 0] Coeff address for C (LSRS) Channel on Main Controller
3Ch	W	7Bh	0Fh	Write [((B0) –1) Biquad 0] Coeff bit [19..16] for C (LSRS) Channel on Main Controller
3Ch	W	78h	1Fh	Write [A2 Biqaud 0] Coeff bit [15..8] for C (LSRS) Channel on Main Controller
3Ch	W	79h	1Fh	Write [A2 Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on Main Controller
3Ch	W	7Ah	47h	Write [A2 Biquad 0] Coeff address for C (LSRS) Channel on Main Controller
3Ch	W	7Bh	07h	Write [A2 Biquad 0] Coeff bit [19..16] for C (LSRS) Channel on Main Controller
3Ch	W	78h	81h	Write [(A1/2) Biquad 0] Coeff bit [15..8] for C (LSRS) Channel on Main Controller
3Ch	W	79h	07h	Write [(A1/2) Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on Main Controller
3Ch	W	7Ah	48h	Write [(A1/2) –1) Biquad 0] Coeff address for C (LSRS) Channel on Main Controller
3Ch	W	7Bh	08h	Write [(A1/2) –1) Biquad 0] Coeff bit [19..16] for C (LSRS) Channel on Main Controller
3Ch	W	78h	81h	Write [(B1/2) Biquad 0] Coeff bit [15..8] for C (LSRS) Channel on Main Controller
3Ch	W	79h	07h	Write [(B1/2) Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on Main Controller
3Ch	W	7Ah	49h	Write [(B1/2) –1) Biquad 0] Coeff address for C (LSRS) Channel on Main Controller
3Ch	W	7Bh	08h	Write [(B1/2) –1) Biquad 0] Coeff bit [19..16] for C (LSRS) Channel on Main Controller
3Ch	W	78h	00h	Write [B2 Biqaud 0] Coeff bit [15..8] for SUB Channel on Main Controller
3Ch	W	79h	6Fh	Write [B2 Biquad 0] Coeff bit [7..0] for SUB Channel on Main Controller
3Ch	W	7Ah	68h	Write [B2 Biquad 0] Coeff address for SUB Channel on Main Controller
3Ch	W	7Bh	00h	Write [B2 Biquad 0] Coeff bit [19..16] SUB Channel on Main Controller
3Ch	W	78h	00h	Write [((B0) –1) Biquad 0] Coeff bit [15..8] for SUB Channel on Main Controller
3Ch	W	79h	70h	Write [((B0) –1) Biquad 0] Coeff bit [7..0] for SUB Channel on Main Controller
3Ch	W	7Ah	69h	Write [((B0) –1) Biquad 0] Coeff address for SUB Channel on Main Controller
3Ch	W	7Bh	08h	Write [((B0) –1) Biquad 0] Coeff bit [19..16] SUB Channel on Main Controller
3Ch	W	78h	ACh	Write [A2 Biqaud 0] Coeff bit [15..8] for SUB Channel on Main Controller
3Ch	W	79h	6Fh	Write [A2 Biquad 0] Coeff bit [7..0] for SUB Channel on Main Controller
3Ch	W	7Ah	6Ah	Write [A2 Biquad 0] Coeff address for SUB Channel on Main Controller
3Ch	W	7Bh	07h	Write [A2 Biquad 0] Coeff bit [19..16] SUB Channel on Main Controller
3Ch	W	78h	2Ah	Write [(A1/2) Biquad 0] Coeff bit [15..8] for SUB Channel on Main Controller
3Ch	W	79h	A7h	Write [(A1/2) Biquad 0] Coeff bit [7..0] for SUB Channel on Main Controller
3Ch	W	7Ah	6Bh	Write [(A1/2) –1) Biquad 0] Coeff address for SUB Channel on Main Controller
3Ch	W	7Bh	08h	Write [(A1/2) –1) Biquad 0] Coeff bit [19..16] SUB Channel on Main Controller
3Ch	W	78h	00h	Write [(B1/2) Biquad 0] Coeff bit [15..8] for SUB Channel on Main Controller
3Ch	W	79h	6Fh	Write [(B1/2) Biquad 0] Coeff bit [7..0] for SUB Channel on Main Controller
3Ch	W	7Ah	6Ch	Write [(B1/2) –1) Biquad 0] Coeff address for SUB Channel on Main Controller
3Ch	W	7Bh	00h	Write [(B1/2) –1) Biquad 0] Coeff bit [19..16] SUB Channel on Main Controller
3Eh	W	78h	36h	Write [B2 Biqaud 0] Coeff bit [15..8] for LSRS Channel on AUX Controller
3Eh	W	79h	33h	Write [B2 Biquad 0] Coeff bit [7..0] for LSRS Channel on AUX Controller
3Eh	W	7Ah	54h	Write [B2 Biquad 0] Coeff address for LSRS Channel on AUX Controller
3Eh	W	7Bh	07h	Write [B2 Biquad 0] Coeff bit [19..16] for LSRS Channel on AUX Controller
3Eh	W	78h	E8h	Write [((B0) –1) Biquad 0] Coeff bit [15..8] for LSRS Channel on AUX Controller
3Eh	W	79h	DFh	Write [((B0) –1) Biquad 0] Coeff bit [7..0] for LSRS Channel on AUX Controller
3Eh	W	7Ah	55h	Write [((B0) –1) Biquad 0] Coeff address for LSRS Channel on AUX Controller
3Eh	W	7Bh	0Fh	Write [((B0) –1) Biquad 0] Coeff bit [19..16] for LSRS Channel on AUX Controller
3Eh	W	78h	1Fh	Write [A2 Biqaud 0] Coeff bit [15..8] for LSRS Channel on AUX Controller
3Eh	W	79h	1Fh	Write [A2 Biquad 0] Coeff bit [7..0] for LSRS Channel on AUX Controller
3Eh	W	7Ah	56h	Write [A2 Biquad 0] Coeff address for LSRS Channel on AUX Controller
3Eh	W	7Bh	07h	Write [A2 Biquad 0] Coeff bit [19..16] for LSRS Channel on AUX Controller
3Eh	W	78h	81h	Write [(A1/2) Biquad 0] Coeff bit [15..8] for LSRS Channel on AUX Controller
3Eh	W	79h	07h	Write [(A1/2) Biquad 0] Coeff bit [7..0] for LSRS Channel on AUX Controller
3Eh	W	7Ah	57h	Write [(A1/2) –1) Biquad 0] Coeff address for LSRS Channel on AUX Controller
3Eh	W	7Bh	08h	Write [(A1/2) –1) Biquad 0] Coeff bit [19..16] for LSRS Channel on AUX Controller
3Eh	W	78h	81h	Write [(B1/2) Biquad 0] Coeff bit [15..8] for LSRS Channel on AUX Controller
3Eh	W	79h	07h	Write [(B1/2) Biquad 0] Coeff bit [7..0] for LSRS Channel on AUX Controller
3Eh	W	7Ah	58h	Write [(B1/2) –1) Biquad 0] Coeff address for LSRS Channel on AUX Controller
3Eh	W	7Bh	08h	Write [(B1/2) –1) Biquad 0] Coeff bit [19..16] for LSRS Channel on AUX Controller



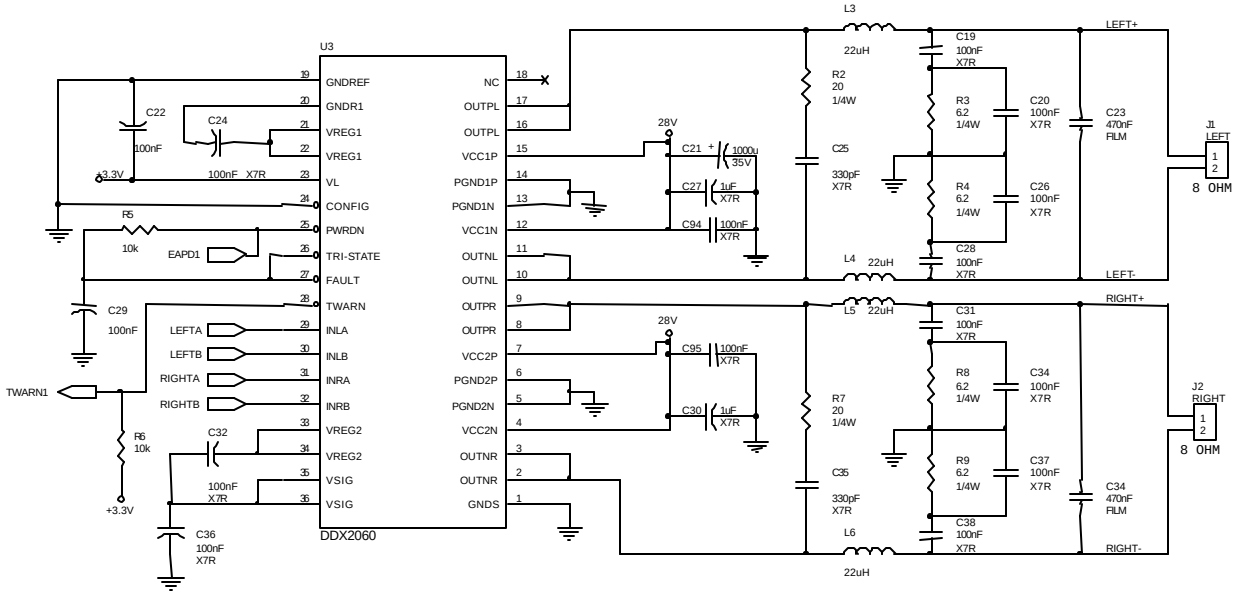
SHEET 1: SYSTEM LEVEL DIAGRAM FOR DESIGN EXAMPLE 1



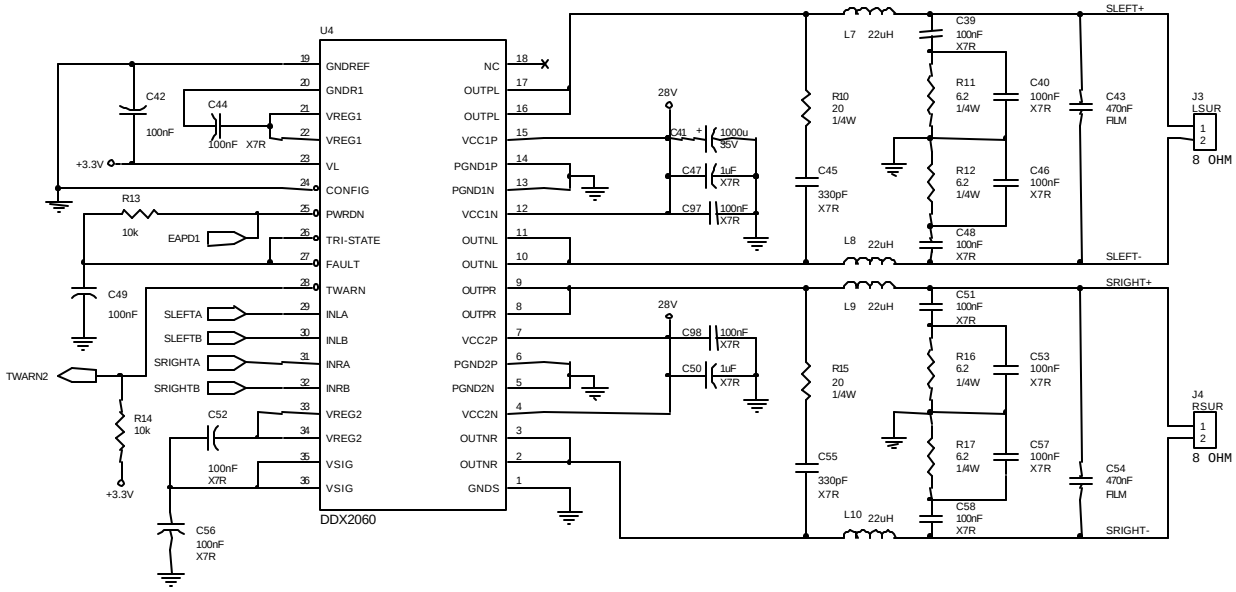
SHEET 2: MAIN DDX-4100 PROCESSOR FOR DESIGN EXAMPLE 1



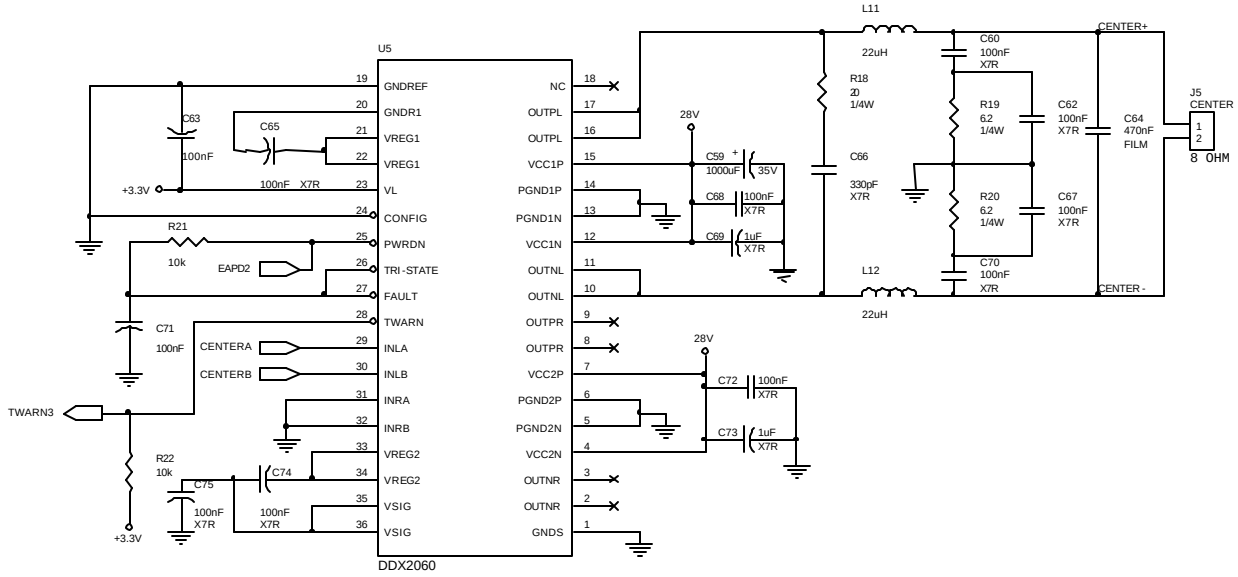
SHEET 3: AUXILIARY DDX-4100 PROCESSOR FOR DESIGN EXAMPLE 1



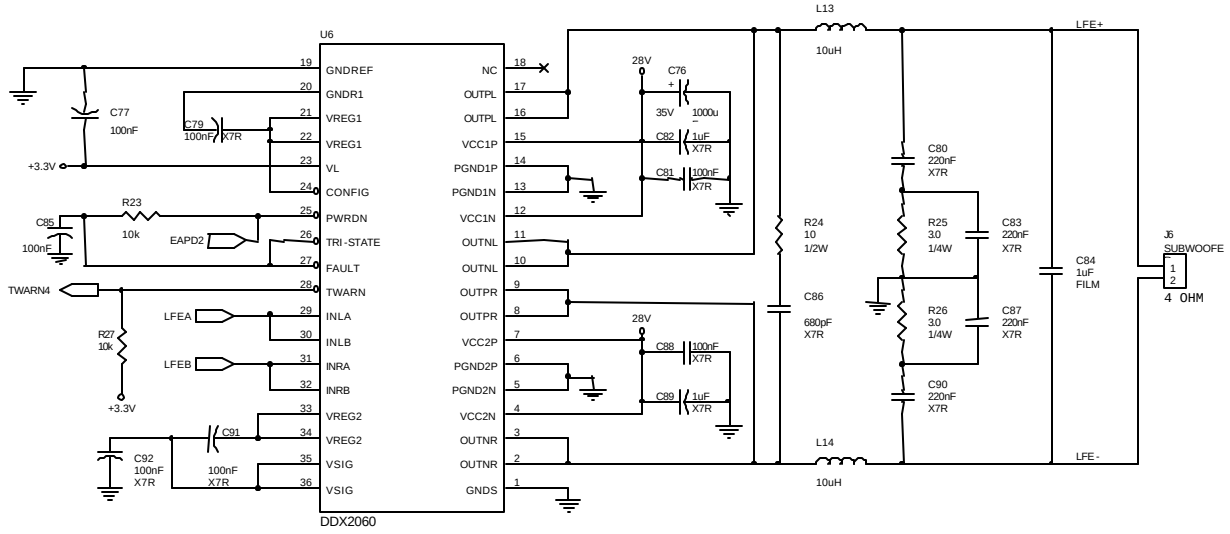
SHEET 4: LEFT AND RIGHT OUTPUTS



SHEET 5: LEFT AND RIGHT SURROUND OUTPUTS



SHEET 6: CENTER OUTPUT



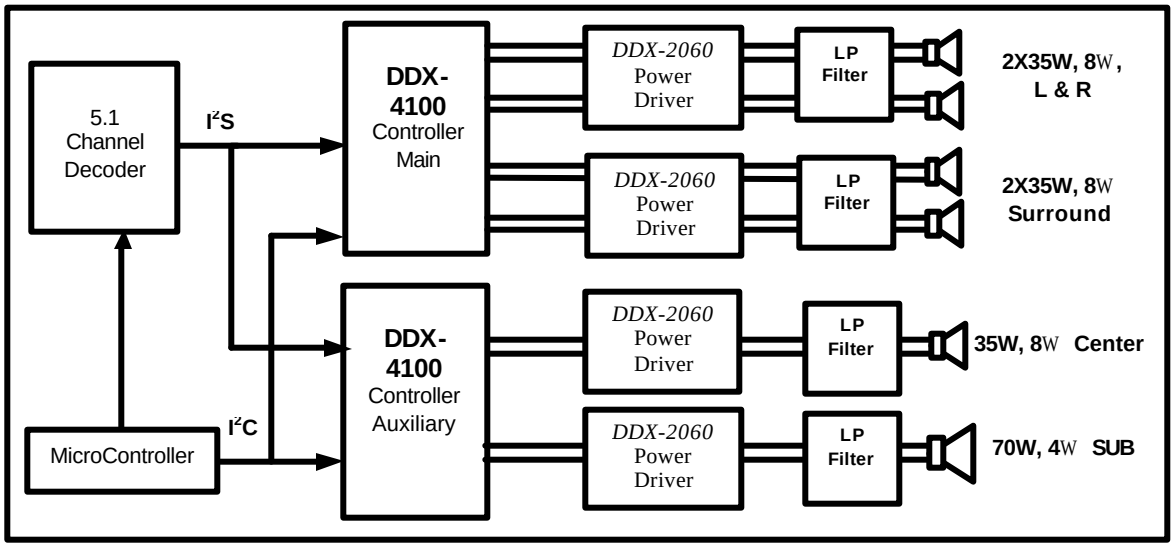
SHEET 7: SUBWOOFER OUTPUT

Design Example 2

Design a DDX 5.1 channel amplifier circuit with 5 x 35W + 1x70W, 6 channel I²S input, MCU control of I²C, and local regulation of logic power supplies. A 5.1 system with I²S inputs are assumed as well as the LFE and CENTER channels are connected to the Aux Controller's Right channel and Left Surround respectively. Below is the Block Diagram and Schematics for the 5.1 system design described above in design example 2.

The Main/Aux Select is done in this example by the micro-controller having two SCL clocks. When using two DDX-4100's in a single system the user must ground SA pin 11 on both ICs, causing both ICs to have the same I²C address = 0x0011110, and use two separate I²C clock pins from the system micro-controller, one for each IC, to address the two processors independently. When communicating with the first processor, the SCL signal connected to the second must remain static and vice versa, refer to DDX-4100 errata at; http://www.apogeeddx.com/ER_DDX_4100.pdf. This setup using one SCL could also be accomplished with a demultiplexer. The micro-controller would provide the Main/Aux Select signal, which would steer the SCL to the correct 4100 as well as the SCL signal, which would be the input into the demux. An example with one SCL is shown in design example one above.

BLOCK DIAGRAM for DESIGN EXAMPLE 2



I²C COMMANDS

The first I²C register settings are used to reset the main and auxiliary ICs. The digital gain is also set to the maximum level for surround sound playback (Digital gain of 9dB or a factor of 3) with compression enabled.

System Reset, Set System Gain

Main/Aux SELECT	R/ W	REG	DATA	COMMENTS
0	W	00h	00h	Soft Reset, Main Controller
0	W	01h	E4h	Soft Reset, Main Controller
1	W	00h	00h	Soft Reset, Auxiliary Controller
1	W	01h	E4h	Soft Reset, Auxiliary Controller
0	W	5Bh	6Dh	Clear DDX Reset, Set DDX Gain=3X, Proprietary (1dB/step)vol. mode, Main
1	W	5Bh	6Dh	Clear DDX Reset, Set DDX Gain=3X, Proprietary (1dB/step)vol. mode, Aux
0	W	26h	00h	Clear EAPD, Main
1	W	26h	00h	Clear EAPD, Aux

***Unmute and Set Desired Channel Volume**

Main/Aux SELECT	R/ W	REG	DATA	COMMENTS
0	W	03h		Set Volume to Desired Setting on Right Channel
0	W	02h		Set Volume to Desired Setting on Left and Unmute Left and Right Channels
0	W	38h		Set Volume to Desired Setting and Unmute Left Surround Channel
0	W	39h		Set Volume to Desired Setting and Unmute Right Surround Channel
1	W	08h		Set Bass/Treble Boost/Cut to Desired Setting (See Appendix D)
1	W	03h		Set Volume on LFE Channel(U2 – Right) to Desired Setting
1	W	02h	3Fh	Unmute LFE Channel(U2 – Right)
1	W	38h		Set Volume to Desired Setting and Unmute Center Channel(U2 – Left Surround)

* When using the sample rate converter (SRC), **it is mandatory to apply a valid input signal to the DDX-4100 prior to unmuting**, refer to DDX-4100 errata at; http://www.apogeeddx.com/ER_DDX_4100.pdf.

BIQUAD Coefficients (Optional)

As an additional example of I²C setting, biquad filters are used to perform speaker equalization and crossover functions. The biquad filters should be written when the devices are muted, i.e., prior to the Unmute commands above.

The biquad coefficients were obtained using Apogee's Filter generation software and were generated in order to equalize a +4dB bump at 2kHz with Q = 1.414 on the L/R/LS/RS/C channels and on the LFE channel a 2nd order Butterworth Low-pass filter with a cutoff of 150Hz was used.

L/R/LS/RS/C Coefficients:

B2: 0x658E0h
(B0)-1: 0xFA043h
A2: 0x5F923h
A1/2: 0x94061h
B1/2: 0x94061h

LFE Coefficients:

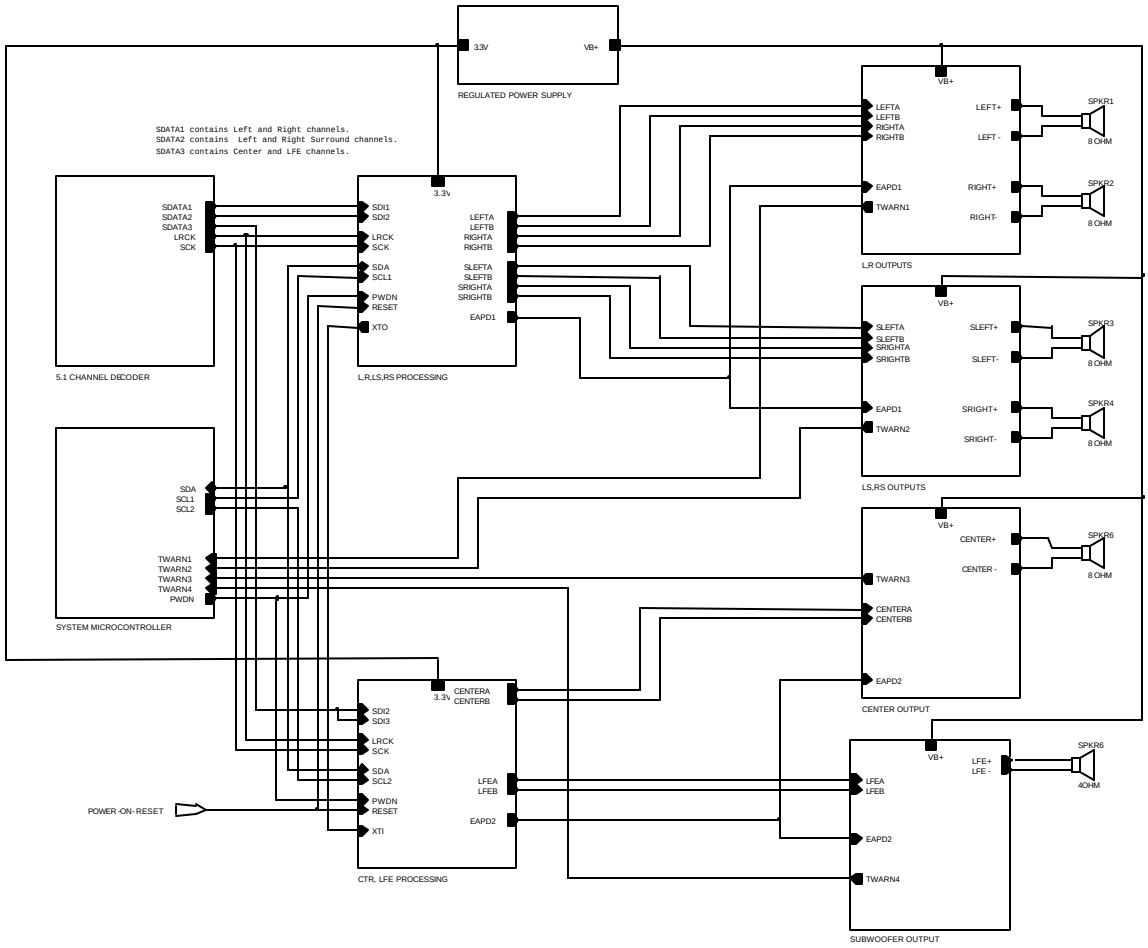
B2: 0x00032h
(B0)-1: 0x80032h
A2: 0x7C7EAh
A1/2: 0x81C6Fh
B1/2: 0x00032h

Following are the steps necessary to write coefficients via I^2C

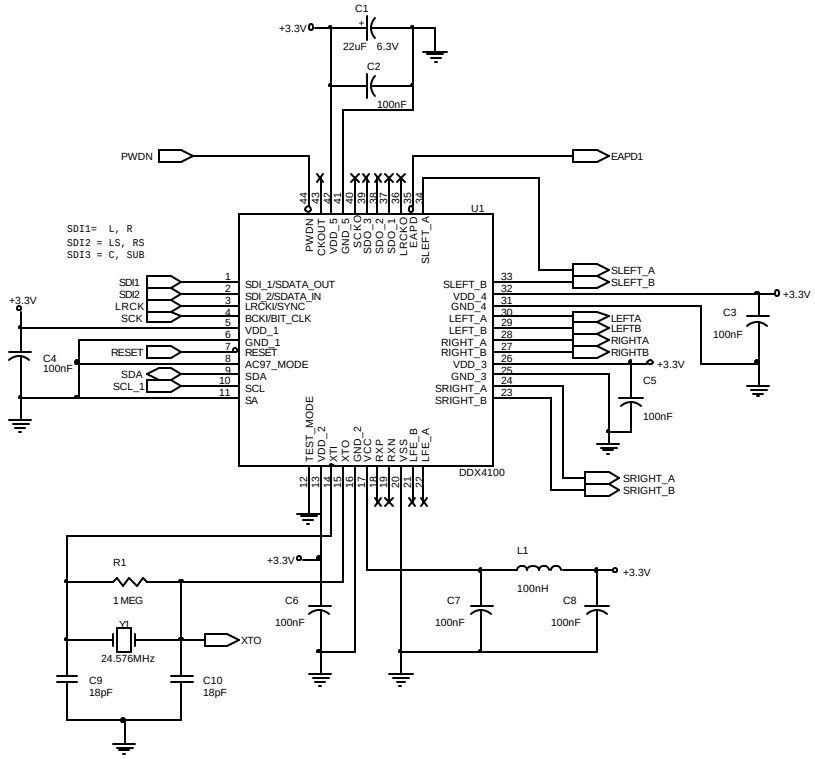
Write 8 middle data bits at I^2C address 78h
Write 8 lower data bits at I^2C address 79h
Write 8 bit address at I^2C address 7Ah coeff INDEX +40h
Write 4 upper data bits and R/W bit at I^2C address

Main/Aux SELECT	R/ W	REG	DATA	COMMENTS
0	W	78h	58h	Write [B2 Biqaud 0] Coeff bit [15..8] for LR Channel on Main Controller
0	W	79h	E0h	Write [B2 Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
0	W	7Ah	40h	Write [B2 Biquad 0] Coeff address for LR Channel on Main Controller
0	W	7Bh	06h	Write [B2 Biquad 0] Coeff bit [19..16] LR Channel on Main Controller
0	W	78h	A0h	Write [((B0) –1) Biquad 0] Coeff bit [15..8] for LR Channel on Main Controller
0	W	79h	43h	Write [((B0) –1) Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
0	W	7Ah	41h	Write [((B0) –1) Biquad 0] Coeff address for LR Channel on Main Controller
0	W	7Bh	0Fh	Write [((B0) –1) Biquad 0] Coeff bit [19..16] LR Channel on Main Controller
0	W	78h	F9h	Write [A2 Biqaud 0] Coeff bit [15..8] for LR Channel on Main Controller
0	W	79h	23h	Write [A2 Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
0	W	7Ah	42h	Write [A2 Biquad 0] Coeff address for LR Channel on Main Controller
0	W	7Bh	05h	Write [A2 Biquad 0] Coeff bit [19..16] LR Channel on Main Controller
0	W	78h	40h	Write [(A1/2) Biquad 0] Coeff bit [15..8] for LR Channel on Main Controller
0	W	79h	61h	Write [(A1/2) Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
0	W	7Ah	43h	Write [(A1/2) –1) Biquad 0] Coeff address for LR Channel on Main Controller
0	W	7Bh	09h	Write [(A1/2) –1) Biquad 0] Coeff bit [19..16] LR Channel on Main Controller
0	W	78h	40h	Write [(B1/2) Biquad 0] Coeff bit [15..8] for LR Channel on Main Controller
0	W	79h	61h	Write [(B1/2) Biquad 0] Coeff bit [7..0] for LR Channel on Main Controller
0	W	7Ah	44h	Write [(B1/2) –1) Biquad 0] Coeff address for LR Channel on Main Controller
0	W	7Bh	09h	Write [(B1/2) –1) Biquad 0] Coeff bit [19..16] LR Channel on Main Controller
0	W	78h	58h	Write [B2 Biqaud 0] Coeff bit [15..8] for LSRS Channel on Main Controller
0	W	79h	E0h	Write [B2 Biquad 0] Coeff bit [7..0] for LSRS Channel on Main Controller
0	W	7Ah	54h	Write [B2 Biquad 0] Coeff address for LSRS Channel on Main Controller
0	W	7Bh	06h	Write [B2 Biquad 0] Coeff bit [19..16] LSRS Channel on Main Controller
0	W	78h	A0h	Write [((B0) –1) Biquad 0] Coeff bit [15..8] for LSRS Channel on Main Controller
0	W	79h	43h	Write [((B0) –1) Biquad 0] Coeff bit [7..0] for LSRS Channel on Main Controller
0	W	7Ah	55h	Write [((B0) –1) Biquad 0] Coeff address for LSRS Channel on Main Controller
0	W	7Bh	0Fh	Write [((B0) –1) Biquad 0] Coeff bit [19..16] LSRS Channel on Main Controller
0	W	78h	F9h	Write [A2 Biqaud 0] Coeff bit [15..8] for LSRS Channel on Main Controller
0	W	79h	23h	Write [A2 Biquad 0] Coeff bit [7..0] for LSRS Channel on Main Controller
0	W	7Ah	56h	Write [A2 Biquad 0] Coeff address for LSRS Channel on Main Controller
0	W	7Bh	05h	Write [A2 Biquad 0] Coeff bit [19..16] LSRS Channel on Main Controller
0	W	78h	40h	Write [(A1/2) Biquad 0] Coeff bit [15..8] for LSRS Channel on Main Controller
0	W	79h	61h	Write [(A1/2) Biquad 0] Coeff bit [7..0] for LSRS Channel on Main Controller
0	W	7Ah	57h	Write [(A1/2) –1) Biquad 0] Coeff address for LSRS Channel on Main Controller
0	W	7Bh	09h	Write [(A1/2) –1) Biquad 0] Coeff bit [19..16] LSRS Channel on Main Controller
0	W	78h	40h	Write [(B1/2) Biquad 0] Coeff bit [15..8] for LSRS Channel on Main Controller
0	W	79h	61h	Write [(B1/2) Biquad 0] Coeff bit [7..0] for LSRS Channel on Main Controller
0	W	7Ah	58h	Write [(B1/2) –1) Biquad 0] Coeff address for LSRS Channel on Main Controller
0	W	7Bh	09h	Write [(B1/2) –1) Biquad 0] Coeff bit [19..16] LSRS Channel on Main Controller
1	W	78h	00h	Write [B2 Biqaud 0] Coeff bit [15..8] for SUB (LR) Channel on AUX Controller
1	W	79h	32h	Write [B2 Biquad 0] Coeff bit [7..0] for SUB (LR) Channel on AUX Controller
1	W	7Ah	40h	Write [B2 Biquad 0] Coeff address for SUB (LR) Channel on AUX Controller
1	W	7Bh	00h	Write [B2 Biquad 0] Coeff bit [19..16] SUB (LR) Channel on AUX Controller
1	W	78h	00h	Write [((B0) –1) Biquad 0] Coeff bit [15..8] for SUB (LR) Channel on AUX Controller
1	W	79h	32h	Write [((B0) –1) Biquad 0] Coeff bit [7..0] for SUB (LR) Channel on AUX Controller
1	W	7Ah	41h	Write [((B0) –1) Biquad 0] Coeff address for SUB (LR) Channel on AUX Controller
1	W	7Bh	08h	Write [((B0) –1) Biquad 0] Coeff bit [19..16] SUB (LR) Channel on AUX Controller
1	W	78h	C7h	Write [A2 Biqaud 0] Coeff bit [15..8] for SUB (LR) Channel on AUX Controller
1	W	79h	EAh	Write [A2 Biquad 0] Coeff bit [7..0] for SUB (LR) Channel on AUX Controller
1	W	7Ah	42h	Write [A2 Biquad 0] Coeff address for SUB (LR) Channel on AUX Controller
1	W	7Bh	07h	Write [A2 Biquad 0] Coeff bit [19..16] SUB (LR) Channel on AUX Controller
1	W	78h	1Ch	Write [(A1/2) Biquad 0] Coeff bit [15..8] for SUB (LR) Channel on AUX Controller
1	W	79h	6Fh	Write [(A1/2) Biquad 0] Coeff bit [7..0] for SUB (LR) Channel on AUX Controller
1	W	7Ah	43h	Write [(A1/2) –1) Biquad 0] Coeff address for SUB (LR) Channel on AUX Controller
1	W	7Bh	08h	Write [(A1/2) –1) Biquad 0] Coeff bit [19..16] SUB (LR) Channel on AUX Controller
1	W	78h	00h	Write [(B1/2) Biquad 0] Coeff bit [15..8] for SUB (LR) Channel on AUX Controller

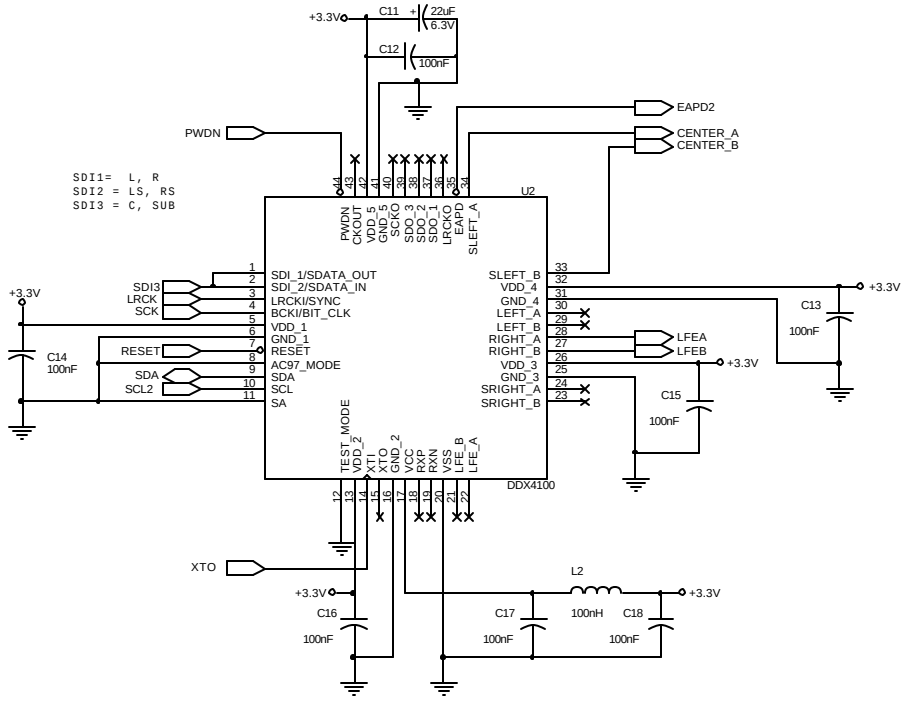
1	W	79h	32h	Write [(B1/2) Biquad 0] Coeff bit [7..0] for SUB (LR) Channel on AUX Controller
1	W	7Ah	44h	Write [(B1/2) –1) Biquad 0] Coeff address for SUB (LR) Channel on AUX Controller
1	W	7Bh	00h	Write [(B1/2) –1) Biquad 0] Coeff bit [19..16] SUB (LR) Channel on AUX Controller
1	W	78h	58h	Write [B2 Biqaud 0] Coeff bit [15..8] for C (LSRS) Channel on AUX Controller
1	W	79h	E0h	Write [B2 Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on AUX Controller
1	W	7Ah	54h	Write [B2 Biquad 0] Coeff address for C (LSRS) Channel on AUX Controller
1	W	7Bh	06h	Write [B2 Biquad 0] Coeff bit [19..16] C (LSRS) Channel on AUX Controller
1	W	78h	A0h	Write [((B0) –1) Biquad 0] Coeff bit [15..8] for C (LSRS) Channel on AUX Controller
1	W	79h	43h	Write [((B0) –1) Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on AUX Controller
1	W	7Ah	55h	Write [((B0) –1) Biquad 0] Coeff address for C (LSRS) Channel on AUX Controller
1	W	7Bh	0Fh	Write [((B0) –1) Biquad 0] Coeff bit [19..16] C (LSRS) Channel on AUX Controller
1	W	78h	F9h	Write [A2 Biqaud 0] Coeff bit [15..8] for C (LSRS) Channel on AUX Controller
1	W	79h	23h	Write [A2 Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on AUX Controller
1	W	7Ah	56h	Write [A2 Biquad 0] Coeff address for C (LSRS) Channel on AUX Controller
1	W	7Bh	05h	Write [A2 Biquad 0] Coeff bit [19..16] C (LSRS) Channel on AUX Controller
1	W	78h	40h	Write [(A1/2) Biquad 0] Coeff bit [15..8] for C (LSRS) Channel on AUX Controller
1	W	79h	61h	Write [(A1/2) Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on AUX Controller
1	W	7Ah	57h	Write [(A1/2) –1) Biquad 0] Coeff address for C (LSRS) Channel on AUX Controller
1	W	7Bh	09h	Write [(A1/2) –1) Biquad 0] Coeff bit [19..16] C (LSRS) Channel on AUX Controller
1	W	78h	40h	Write [(B1/2) Biquad 0] Coeff bit [15..8] for C (LSRS) Channel on AUX Controller
1	W	79h	61h	Write [(B1/2) Biquad 0] Coeff bit [7..0] for C (LSRS) Channel on AUX Controller
1	W	7Ah	58h	Write [(B1/2) –1) Biquad 0] Coeff address for C (LSRS) Channel on AUX Controller
1	W	7Bh	09h	Write [(B1/2) –1) Biquad 0] Coeff bit [19..16] C (LSRS) Channel on AUX Controller



SHEET 1: SYSTEM LEVEL DIAGRAM FOR DESIGN EXAMPLE 2



SHEET 2: MAIN DDX-4100 PROCESSOR FOR DESIGN EXAMPLE 2



SHEET 3: AUXILIARY DDX-4100 PROCESSOR FOR DESIGN EXAMPLE 2

L/R OUTPUTS: Refer to SHEET 4 (LEFT AND RIGHT OUTPUTS)

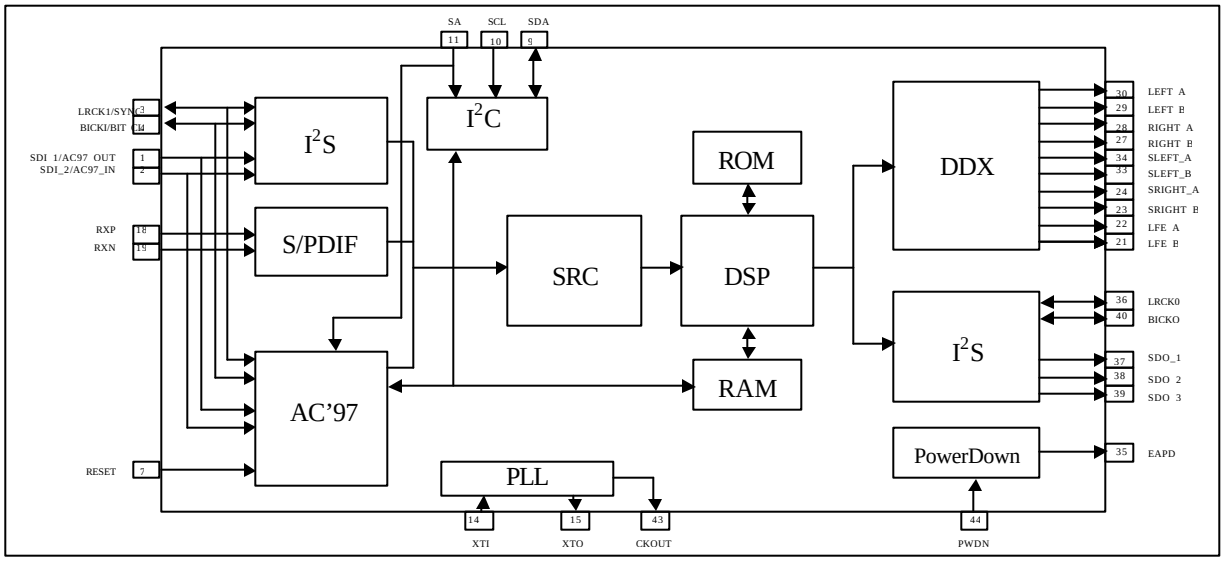
L/R SURROUND OUTPUTS: Refer to SHEET 5 (LEFT AND RIGHT SURROUND OUTPUTS)

CENTER OUTPUT: Refer to SHEET 6 (CENTER OUTPUT)

SUBWOOFER OUTPUT: Refer to SHEET 7 (SUBWOOFER OUTPUT)

Appendix A
DDX-4100 Overview

Provided is an overview of the DDX-4100 for quick references but, it is suggested that the user be familiar with the DDX-4100 Datasheet prior to proceeding. The DDX-4100 Digital Audio Processor performs preamplifier functions between the digital audio data input and the DDX power devices as shown in Figure 1. The processor supports two input configurations; AC'97 input mode or Serial/SPDIF input mode, with the selection made via a dedicated pin.



DDX-4100 Block Diagram- Figure 1

Digital Audio Inputs

In the Serial/SPDIF mode, a stereo S/PDIF or a 4 channel three-wire programmable serial input interface supports any sampling frequency in the continuous range from 32 to 96 KHz. The programmable serial interface supports up to four channels as two synchronized stereo data steams. It accepts all common formats including the popular IIS protocol. Operation of the S/PDIF or the Serial inputs is mutually exclusive. The SPDIF input routes its 2 channels to the left and right channels within the DDX-4100. The serial interface routes its 4 channels to the left, right, left surround, and right surround channels. In the design examples only the serial interface is used.

The AC'97 interface, mainly used on PC motherboards, is compliant with 'Audio Codec '97 – Revision 2.1' specification in terms of the protocol used. AC'97 is not covered in this application note. For AC'97 applications assistance contact Apogee Technical Support at; http://www.apogeeddx.com/apogee_form.html.

I^2C

The DDX-4100 provides an I^2C control interface. This interface must be connected to the system micro-controller for control of the DDX-4100. The DDX4100 will operate only in slave mode. For specifics of the I^2C protocol refer to the DDX-4100 datasheet and DDX-4100 errata.

Sample Rate Converter

The first processing block reached by the signal in the DDX4100 is the sample rate converter (SRC). The SRC resamples all incoming data to a constant output sample rate regardless of the input sample frequency. This sample rate is determined by the internal master clock and will be 48kHz when using the recommended 24.576MHz crystal. The SRC can handle input sample rates of 32kHz to 96kHz. It is required when using the SRC to disable the double buffering feature via configuration register A. It is also mandatory to apply a valid input signal to the DDX 4100 prior to unmuting. Note that the SRC lock indicator, (register 0x77, bit 0), incorrectly shows SRC lock valid at power up even with no signal applied, refer to DDX4100 errata at; http://www.apogeeddx.com/ER_DDX_4100.pdf.

DSP

The DDX4100 contains a fixed function 20-bit audio DSP (Figure 2 is an example of the digital audio signal flow in the DSP). This DSP performs the functions of tone control, programmable EQ, and volume control. The output of the DSP goes to the serial output ports and to the DDX blocks.

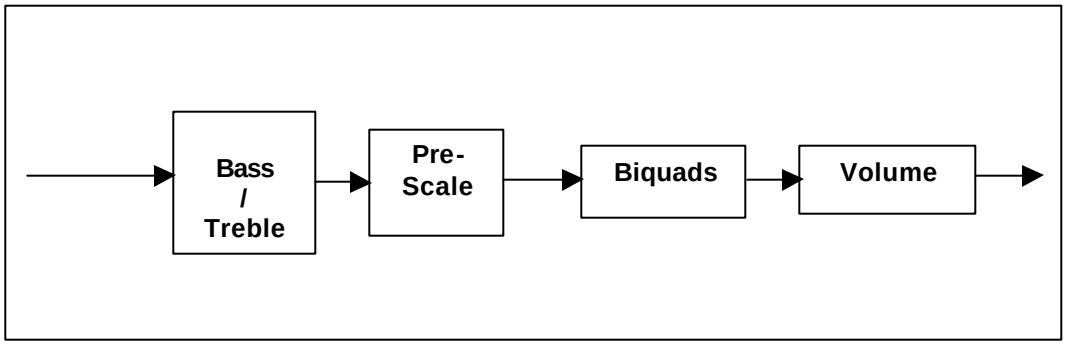


Figure 2: Signal Flow in the DSP

The bass/treble tone controls only affect the inputs on the SDI_1 pin. When boosting using the bass/treble controls it becomes possible to clip the input signal. This is because the volume control is positioned after the bass/treble functionality. To avoid this possibility it is necessary to attenuate the input signal to the DDX-4100. In Appendix C more information on how to prevent clipping is provided. The programmable EQ allows download of user generated coefficients from a micro-controller and can generate high and low-pass filters for crossover and parametric filters for frequency response adjustment. Apogee provides a graphical interface filter generation software for generating coefficients formatted for downloading to the DDX4100. Detailed design information for filters supported by the DDX-4100 can be found at; http://www.apogeeddx.com/BQD_Appnote.PDF. The volume controls are independent per channel.

DDX

The DDX processing in the DDX-4100 converts the incoming 48kHz PCM data streams into a high-quality 384kHz DDX pulse width modulated (PWM) signals to drive the power devices

Software Control

Using the I^2C interface to write to internal registers controls the functionality of the DDX-4100. Table 1 shows an overview of the registers and their respective purpose. When using serial or SPDIF input, I^2C is the control interface and the registers are 8-bits wide with every address being used.

Table 1
DDX-4100 Registers

DDX-4100 Datasheet Paragraph	Register Name	Serial / S/PDIF	AC'97[1]	Comments
12.1	RESET	00,01	00	Sets all registers to their default values.
12.2	LRVOL	02,03	02	Unmute and sets Left & Right volume levels
12.3	TONE	08,09	08	Sets Bass and Treble levels on Left & Right Channels
12.4	POWER-DOWN	26	26	Power-Down controls for internal clock and volume fade-out and mute.
12.5	AUDIO ID	N/A	28	Identifies Extended Audio Features (AC'97 only)
12.6	AUDIO STATUS	N/A	2A	Read-Only Extended Audio Feature Readiness (AC'97 only)
12.7	SAMPLE RATE	N/A	2C-34	Sample Rate Control Registers (AC'97 only)
12.8	6 CHNL. VOLUME	36,38,39	36,38	Mute and Volume control for LFE, Center (AC'97 only), Left Surround and Right Surround Channels.
12.9	CRA	5A, 5B	5A	Configuration Register A: Control of AC'97, Double Buffer Mode, DDX Gain, Reset, Zero Detect and Power Mode, PLL factor and Bypass, MCKOut, I2S.SPDIF Select, SRC Threshold, DRLL Debug Mode and SRC Bypass.
12.10	CRB	5C, 5D	5C	Configuration Register B: Control of I2S Input Alignment, BICK Polarity, BiCKI/BICKO and LRCKI/LRCKO Master/Slave, LRCKI/LRCKO Polarity, Input/Output MSB/LSB Select, I2S Output Alignment
12.11	PHANTOM	N/A	60	Phantom Center Channel Enable (AC'97 only)
12.12	STATIC EQ / SIDE	71	70	Enable Static EQ and/or Side-Firing Surround Channels.
12.13	BASS MGMT	73	72	Enable Bass Management (Mix 6 channels to SBW)
12.14	BYPASS	75	74	Bypass DSP block
12.15	BASR	77	76	BIST and Status Register; Read SRC and S/PDIF Lock, Auto-Mute on AC3 Frame Header or no CH1_STATUS
12.16	COEFFS	78,79, 7A,7B	78,7A	EQ and Bass Management Coefficients and Scale Factors
12.17	VENDOR ID	7C,7D, 7E,7F	7C,7E	Vendor Ids, Read-Only.

Appendix B

5.1 Channel Power Configurations Using the DDX-2060 and DDX-2100 Power Devices

There are several different 5.1 channel system configurations possible using the DDX chip set solution. For example, the block diagram for Design 1 demonstrates a solution that provides 5x35W plus 1x70W using two DDX-4100 devices and four DDX-2060 power devices. Since the DDX power devices can be configured in stereo or signal channel mode multiple configurations can be implemented to provide to meet the power output requirements of the system. As an example, eight configurations are shown below using the DDX-2060 and DDX-2100 power devices.

5.1 Channel System Configurations

Output Power Configuration*	Speaker Impedance	# Devices	Device Output Configuration
6x35W	8 Ohms	3 DDX-2060's	Two channel
5x35W + 1x70W	8 Ohms 4 Ohms	3 DDX-2060's 1 DDX-2060	Two channel Mono
6x70W	4 Ohms	6 DDX-2060's	Mono
5x70W+ 1x140W	4 Ohms 2 Ohms	5 DDX-2060's 2 DDX-2060's	Mono Mono Combined
6x50W	8 Ohms	3 DDX-2100's	Two channel
5x50W+ 1x100W	8 Ohms 4 Ohms	4 DDX-2100's 1 DDX-2100's	Two channel Mono
6x100W	4 Ohms	6 DDX-2100's	Mono
5x100W+ 1x200W	4 Ohms 2 Ohms	5 DDX-2100's 2 DDX-2100's	Mono Mono Combined

*Using a supply voltage of +28 VDC for the DDX-2060 and +36 VDC for the DDX-2100.

The system configuration power is determined by the supply voltage, the speaker impedance, the capabilities of the power device and how the power devices is configured (i.e., two channel, mono or mono combined). Lower power outputs can be obtained in each of these configurations if needed by reducing supply voltage or increasing speaker impedance. http://www.apogeeddx.com/Apogee_01_applications.PDF contains more detailed information , specifically, graphical plots of power output vs. speaker impedance and voltage are provided.

If a power amplifier is required for the subwoofer channel, typically referred to as the .1 channel, it is generally advantageous that this channel provide a higher power output. The original intention of the .1 channel was to provide more headroom at low-frequencies. Higher output from the subwoofer speaker compared to the other speaker outputs is suggested for proper playback of surround sound material.

Appendix C
Avoiding Signal Clipping when Using Bass/Treble Gain

The DDX-4100 includes a bass/treble function that can be set between +/- 12 dB of gain using the I^2C registers. In cases where the input signal level to the bass/treble block is above –12dB and the bass/treble settings are above 0 dB, signal clipping can occur. In order to best utilize this function, pre-scaling can be performed using the volume control in the surround decoder. When combined with the DDX-4100 volume control the overall desired system gain can be implemented. The table below shows the Decoder and DDX-4100 volume control registers for a given desired overall system volume.

MASTER VOLUME TABLE

Desired System Volume Setting	Decoder Volume Setting	DDX-4100 Volume Setting
0dB	0dB	0dB
-1dB	-1dB	0dB
-2dB	-2dB	0dB
:	:	:
-11dB	-11dB	0dB
-12dB	-12dB	0dB
-13dB	-12dB	-1dB
:	:	:
-29dB	-12dB	-17dB
-30dB	-12dB	-18dB
:	:	:

Appendix D
Using Volume Offsets to Increase Relative Gain on the Subwoofer Channel

It is suggested to have a volume level "offset" for the Subwoofer Channel. It is also recognized that a higher overall maximum gain is often needed for the subwoofer channel. Using Design 2 as an example we can accomplish this by using the Bass/Treble boost feature on the Subwoofer channel. In the auxiliary DDX-4100, Bass(U2), is used to add the desired gain to the subwoofer channel, the Subwoofer Offset Volume Table demonstrates this below.

SUBWOOFER OFFSET VOLUME TABLE

System Volume Setting	Decoder Volume Setting	Main 4100 Volume Setting	Aux 4100 Volume Setting	BASS(U2) Bass/Treble Boost/Cut Setting
0dB	0dB	0dB	0dB	+6dB
-1dB	-1dB	0dB	0dB	+6dB
:	:	:	:	:
-11dB	-11dB	0dB	0dB	+6dB
-12dB	-12dB	0dB	0dB	+6dB
-13dB	-12dB	-1dB	0dB	+5dB
:	:	:	:	:
-18dB	-12dB	-6dB	0dB	0dB
-19dB	-12dB	-7dB	-1dB	0dB
:	:	:	:	:
-29dB	-12dB	-17dB	-11dB	0dB
-30dB	-12dB	-18dB	-12dB	0dB
:	:	:	:	:

Note that the Main 4100 drives L,R,LS and RS Channels and the Aux 4100 drives Center and Sub Channels.