Applying the DDX-8000 in Binary Mode

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1. Introduction

With the release of the DDX-8000 Digital Audio Processor, it is possible to operate in a single-ended binary mode, or differential DDX ternary mode. Binary Mode enables up to four output channels per power device (DDX-2060 and DDX-2100), which is double the channels available with DDX ternary operation. System complexity and cost are thus reduced. This Note will clarify several important points to assure a successful Binary mode design using Apogee Technology's DDX devices.

1.1. Binary compared to Ternary system: Advantages and Disadvantages

1.1.1. Binary Advantages

- Reduced system cost
- Simpler, smaller design, lower parts count

1.1.2. Binary Disadvantages

- Less available power per channel
- Lower SNR
- Higher crosstalk
- Less "Pop" Immunity

1.2. Reference Designs (see Section 6 for schematics)

Two of the most popular amplifier configurations are 2.1ch (Left, Right and Subwoofer channels for stereo programs) and 5.1ch (Left, Right, Center, Left Surround, Right Surround and Subwoofer channels for Surround Sound programs). Three designs are considered in Section 6; two 5.1ch and one 2.1ch. The first design is 5.1ch with channel layout L/R/LS/RS from the first power device, Ctr and Sub from the second. This design is realized in reference board RB-86125, available from Apogee. The second design is also 5.1ch. The channel layout provides operation flexibility in channels used, so that when the amplifier is operated as a 2.1ch, the second power device is disabled by the system MCU with the EAPD1 signal. This assures that only the L, R and Sub channels are active and no hiss or noise can be produced by the unused LS, RS and Ctr channels. The third design is a 2.1ch using a single power device.

2. Filter Components

DDX-2060/2100 Binary Filter Component Values

LS1	**8Ω**	**6Ω**	**4Ω**
L1	**47µH**	**33µH**	**22µH**
C1	**390nF**	**470nF**	**680nF**
R1,2	**6.2kΩ**	**4.7kΩ**	**3.4kΩ**
C2	**180µF**	**220µF**	**330µF**

Table 1: Binary Filter Component Values

Notes:

1. C2 is determined using the formula **C2** = **1/(2π*f_{3dB}*Z_{spkr})** with f_{3dB} =120Hz.
2. C2 requires time to be charged to operating voltage before applying the output section to the speaker. If the speaker is connected before C2 is charged, the difference between the uncharged capacitor voltage and the operating voltage will cause an audible "POP" at the speakers. For no "POP" on start-up, the 2060 or 2100 power device is muted for 2 or more RC Time Constants, where **R= R1** and **C= C2.** This delay is performed by the DDX-8000 or system MCU.

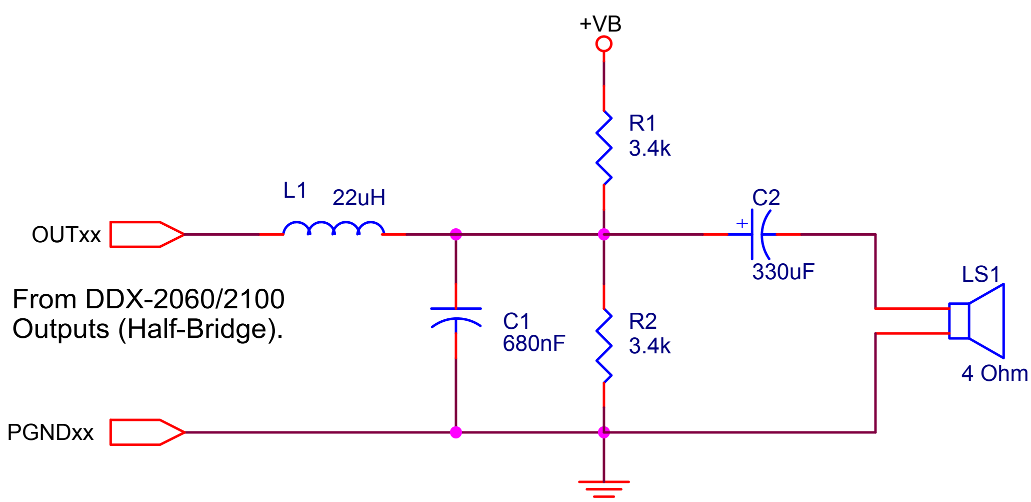

Figure 1. Binary Output Filter

For improved crosstalk performance, C2 can be 'split' into two capacitors, one connecting to VB and one to ground as seen in Figure 2. C2 and C3 are 82µF for 8Ω speakers, 100µF for 6Ω speakers and 180µF for 4Ω speakers.

LS1	8Ω	6Ω	4Ω
L1	47µH	33µH	22µH
C1	390nF	470nF	680nF
R1,2	6.2kΩ	4.7kΩ	3.4kΩ
C2,3	82µF	100µF	180µF

Table 2: Modified Binary Filter Component Values

Note:
1. For no "POP" on start-up, the 2060 or 2100 power device is muted for 4 or more RC Time Constants, where R= **R1** and C= **C2.** This delay is performed by the DDX-8000 or system MCU.

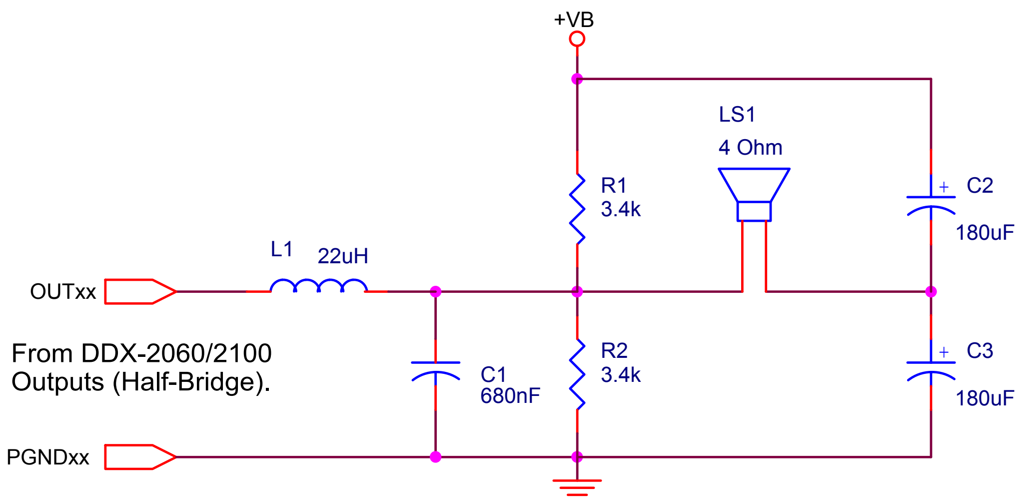

Figure 2. Binary Output Filter with Crosstalk Improvement Modification

3. Design Considerations

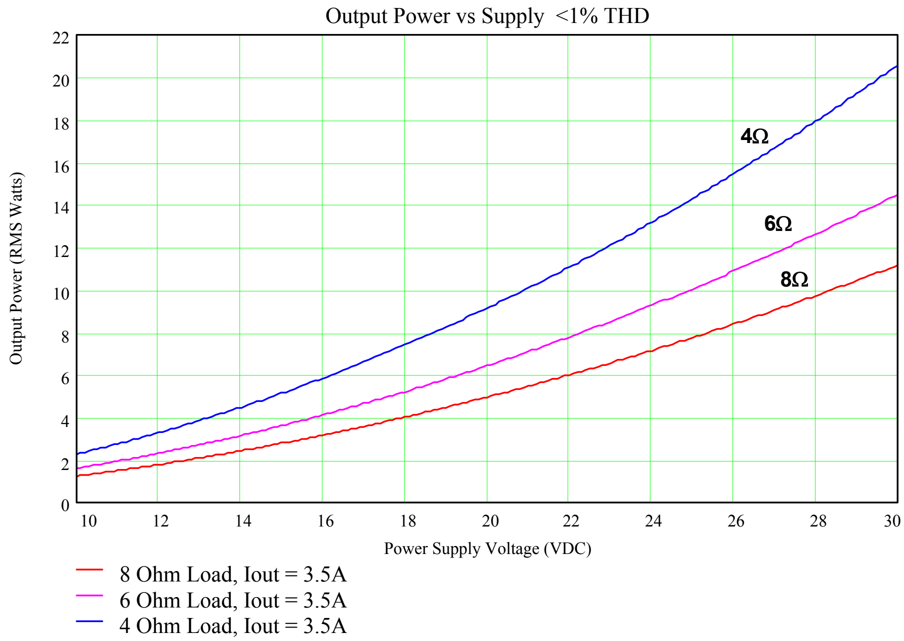

Figure 3. Output Power, Low THD+N

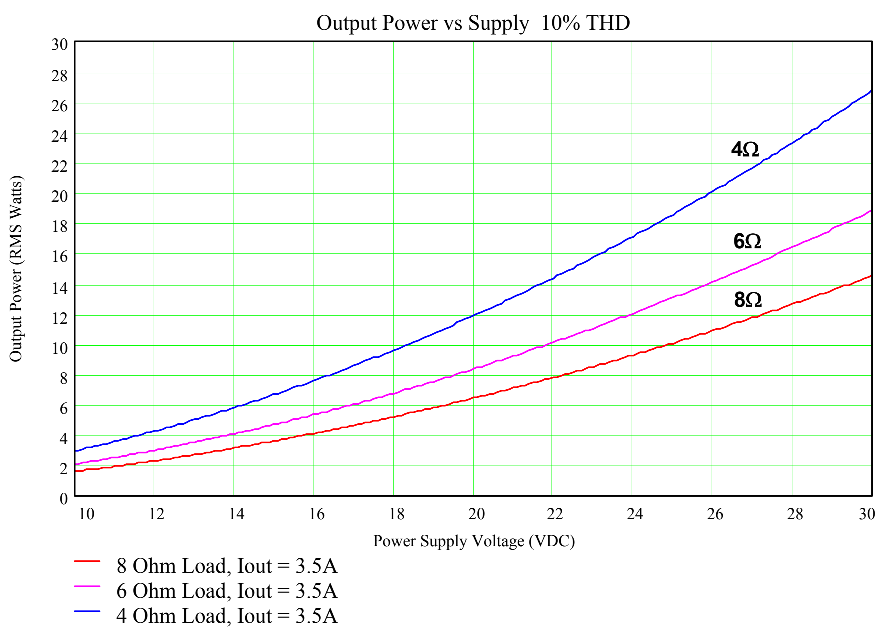

Figure 4. Output Power, 10% THD+N

3.1. Clocking:

When any of the PWM outputs are used in Binary Mode it is important that the proper steps be taken in order to eliminate or minimize the level at which a pop can be generated from the power stage. In the Binary Mode pops can occur when the Input clocking (MCLK, LRCLK, or BCLK) are changed or lost. Clock changes and Clock Losses can occur when there are changes between sources (changes between DVD, CD, Analog or any input source via a MUX interfaced to the DDX-8000) or when the device/s interfacing to the DDX-8000 can not provide a constant or stable clock source. This can cause the loss of either one or all of the serial clock inputs to the DDX-8000 (MCLK, LRCLK or BCLK) depending on various MPEG, SPDIF, or Audio Decoder Devices.

In a system, in which input clocks become unstable because of source switching, the MCU is always aware of changes between audio sources. When a change occurs the MCU must perform the following steps in-order to ensure that the pops be eliminated or minimized when a change in source occurs.

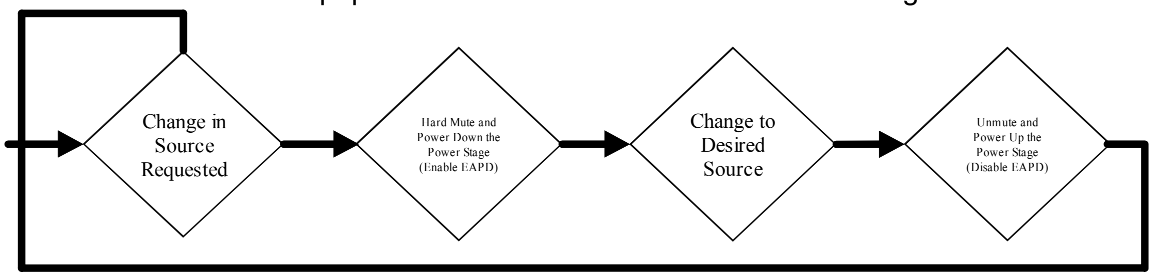

Figure 5. Required MCU steps to eliminate POP caused by clock changes

4. Layout Requirements and Recommendations

The placement of Power supply bypass capacitors for the DDX-2060 or DDX-2100 is very critical and we recommend following our Reference Board Designs exactly for these capacitors location & tracking. Figure 6, Figure 7 and Figure 8 are shown here for reference, however it is suggested to take a close look at the PCB Gerber files and actual reference PCB before starting the PCB layout.

There are 3 types of capacitors used for Power supply bypassing as follows,

a) **Bulk Bypass**: This is normally an aluminum electrolytic type with the value 1000uF/35V(DDX-2060), or 1000uF/50V(DDX-2100), 20% tolerance (C27 in the picture below). The placement is less critical but the traces supplying the power to the DDX chip is routed thru this capacitor, thus the traces must be routed directly to the power device.

b) **HF bypass**: This is normally a Multilayer ceramic chip type SMD package with value 100nF, X7R, 10%. (C37 & C42 in the figures below) The placement of this capacitor is very critical. It is recommended to follow exact placement & tracking as per our Reference PCB Designs. The GND connection trace must be connected directly to DDX-2060/2100 GND pins on component layer copper from at least one of the HF bypass capacitors.

c) **HF bypass**: This is normally a tantalum capacitor in SMD package with the value of 1uF, 10% (C33 & C40 in the figures below). This is also very critical in terms of placement & highly recommended to follow the Apogee Ref PCB design. If Tantalum type can't be used then Multilayer Ceramic Chip X7R type with SMD package can be substituted. Aluminum electrolytic will not work at these locations due to high frequency operation.

d) **Speaker Ground return**: For crosstalk reduction, it is imperative to provide short, direct paths from the speaker's ground connection to the Bulk Bypass capacitor and PGND pins of the power device.

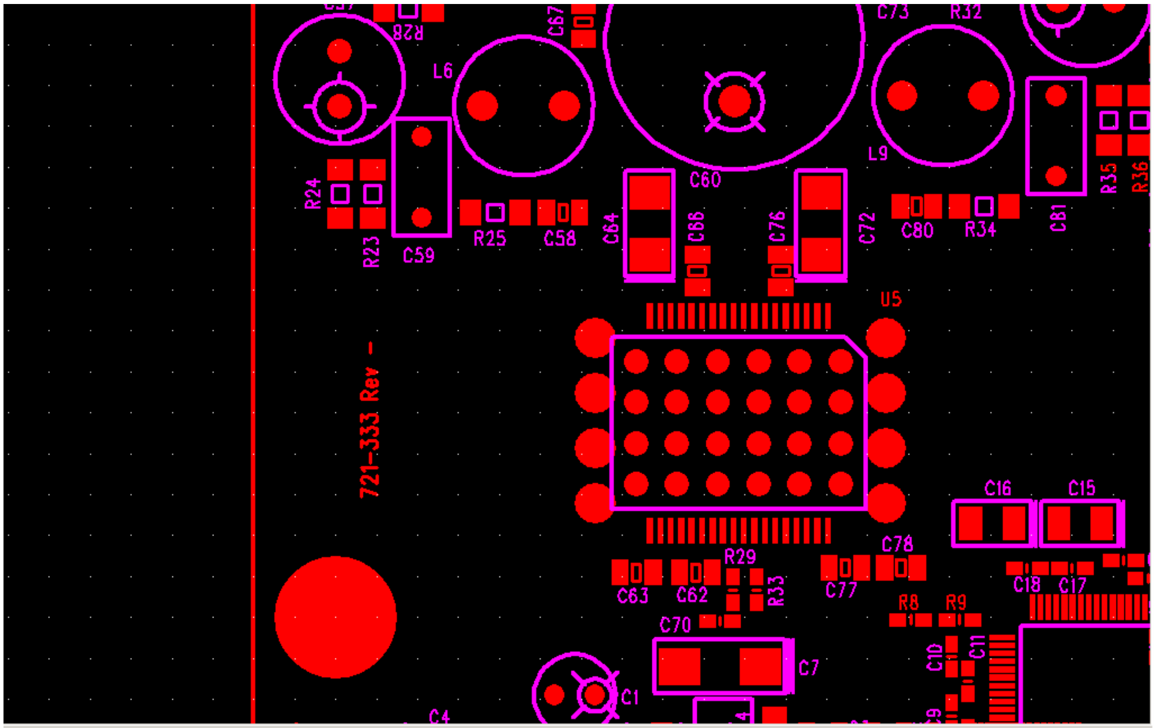

Figure 6. Component (top) Side Component Placement

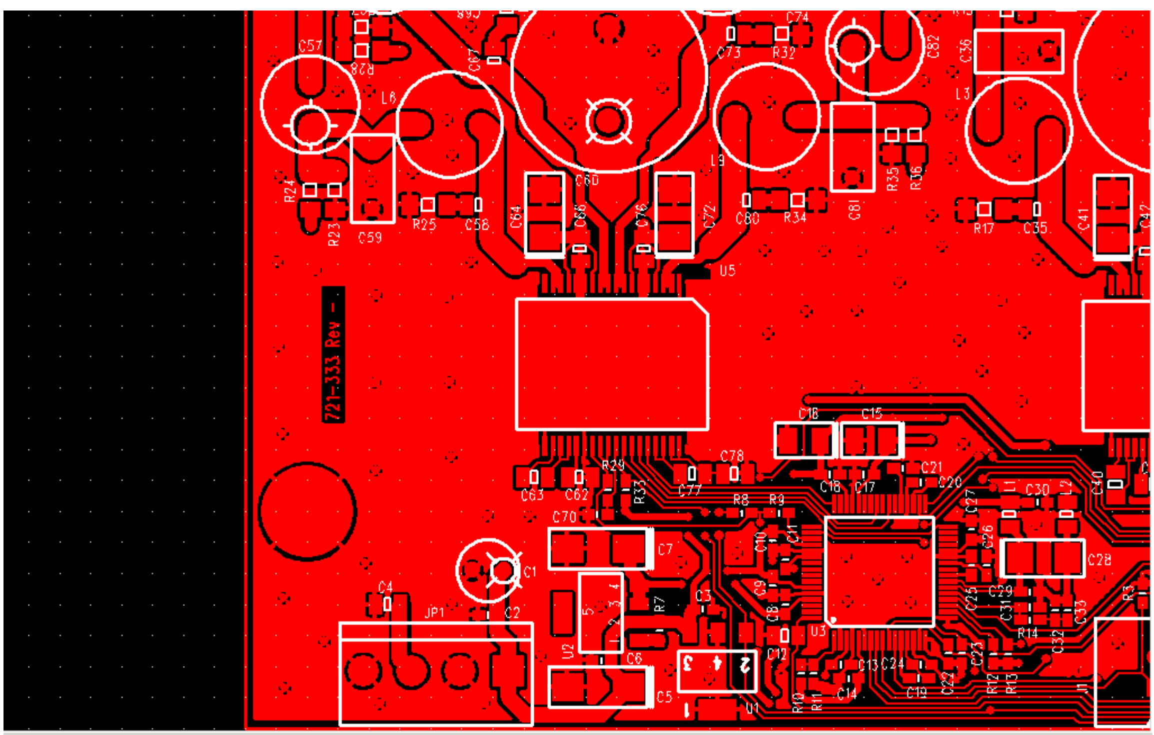

Figure 7. Component Side Copper Layout

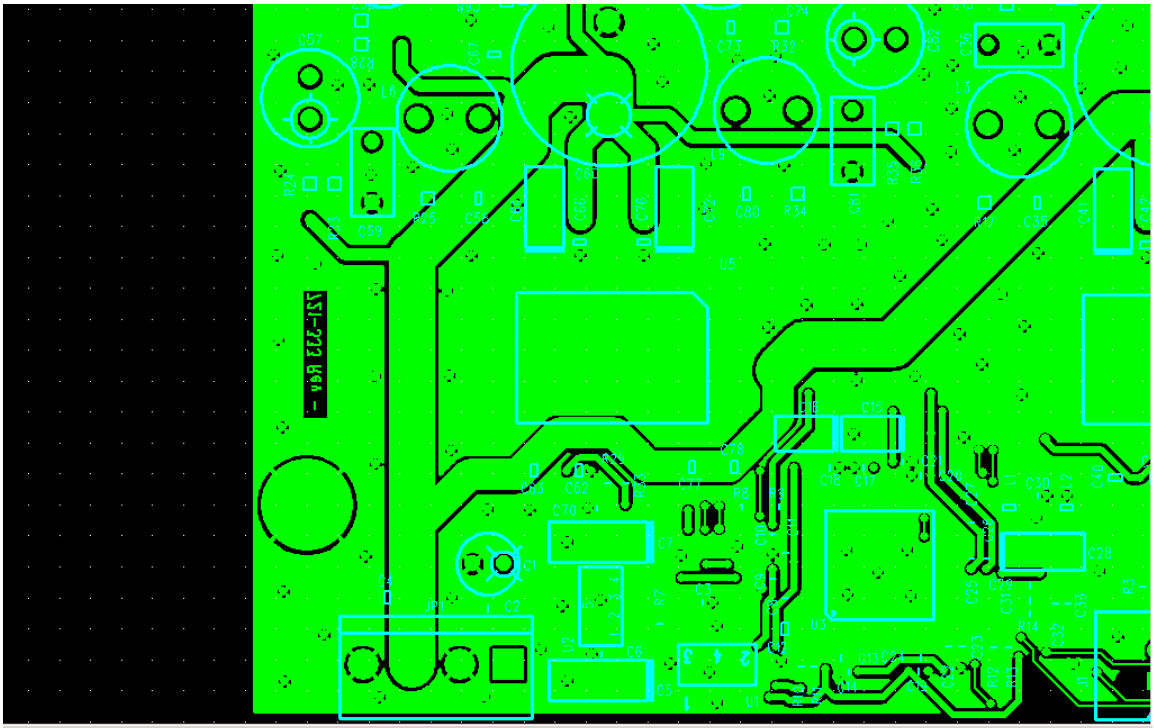

Figure 8. Copper (bottom) Side Copper Layout

5. DDX-8000 Programming Guidelines

5.1. Channel Mapping:

Several differences exist between software control of the DDX-8000 for ternary(DDX) operation and binary operation. First and most importantly is the need to map channels internally for best performance. This is accomplished using the channel mapping feature of the DDX-8000. It must be remembered that the channel mapping feature occurs first in the signal processing chain and therefore all other operations will need to account for the mapping of the channels.

As an example here is a block diagram of the inputs and outputs for a binary set-up consistent with the RB-86125 Reference Board. The actual channels at the input and output can be changed from this example for certain designs. But it is very important for performance that the outputs shown are used and that they are assigned to the DDX-2060/2100 in the manner described in this AppNote.

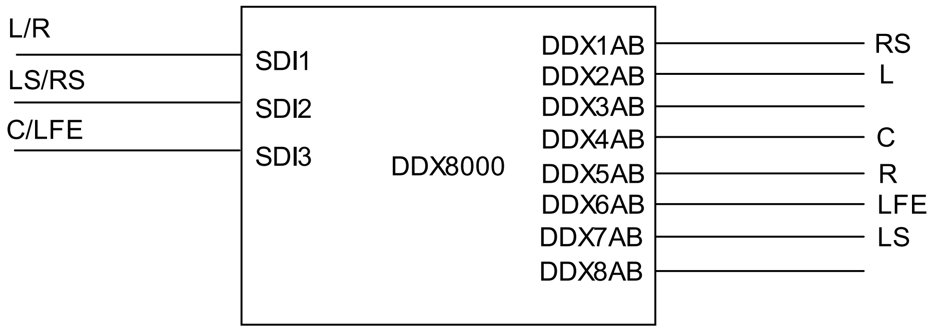

Figure 9. RB-86125 Reference Board channel map

To perform this channel mapping via I2C;

Register Address	Register Data	Comment
11h	00000011b	Map In4 > Out1, Map In1 > Out2
12h	0100xxxxb	Map In5 > Out4
13h	01010001b	Map In2 > Out5, Map In6 > Out6
14h	xxxx0010b	Map In3 > Out7

5.2. Other Initialization:

Other initialization and settings can be performed consistently with ternary DDX-8000 applications with the exception that channels will be different internally because of the channel mapping performed. Note that I2S outputs follow output channel mapping selections.
Please refer to AppNote***: I²C Procedure For 5.1 Applications Using the DDX-8000***.

5.3. Start-Up:

To prevent a "pop" sound at start in a binary system it is necessary to let the output bias voltage charge. This requires a delay at start-up before the power devices are turned on and the DDX8000 is un-muted. Therefore after initialization is performed the following steps should be taken. The wait state can be adjusted depending on the individual system.

Register Address	Register Data	Comment
03h	xxxx1111b	Set All Channels to Binary Output
Wait	Wait	Wait State for ~2.5s
05h	10000000b	Configuration Register F, Set EAPD
07h	xxxxxxxxb	Unmute, Set Master Volume

5.4 Source Switching

During source switching it may be necessary to disable the power devices to insure that no "pop" sounds occur at the speaker output. This is accomplish by first hard muting the device, then powering down the power devices via EAPD before the clocks become unstable.

Register Address	Register Data	Comment
07h	11111111b	Set Master Hard Mute
05h	0xxxxxxxb	EAPD
		Source Switching
05h	1xxxxxxxb	unEAPD
07h	xxxxxxxxb	Reset Master Volume Setting

Reference Schematics

5.4. 5.1ch Schematic; 2/4/5/7, 1/6 (L/R/LS/RS, CTR/SUB as realized in RB-86125)

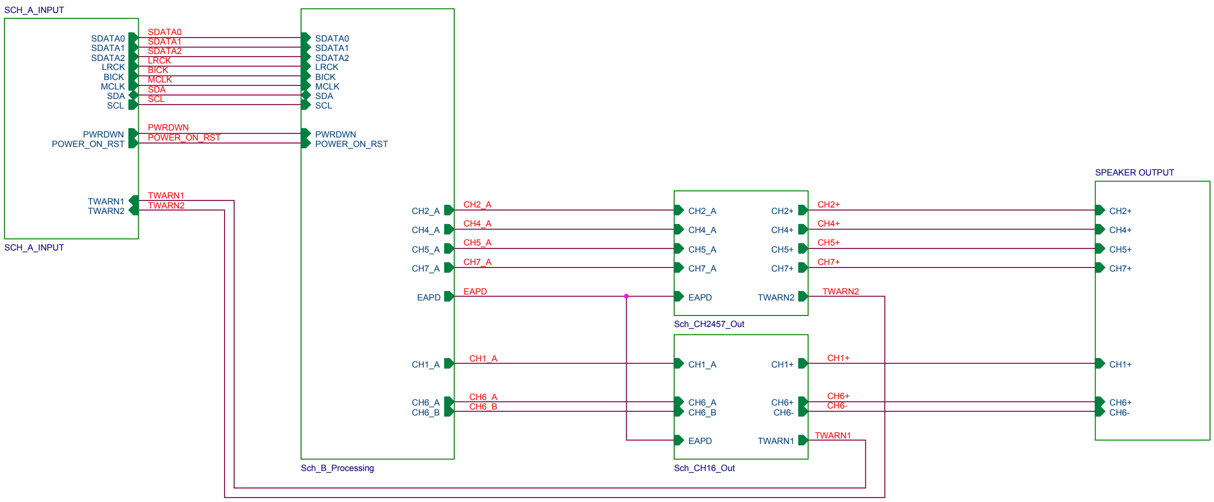

Figure 10. 5.1ch Block Diagram

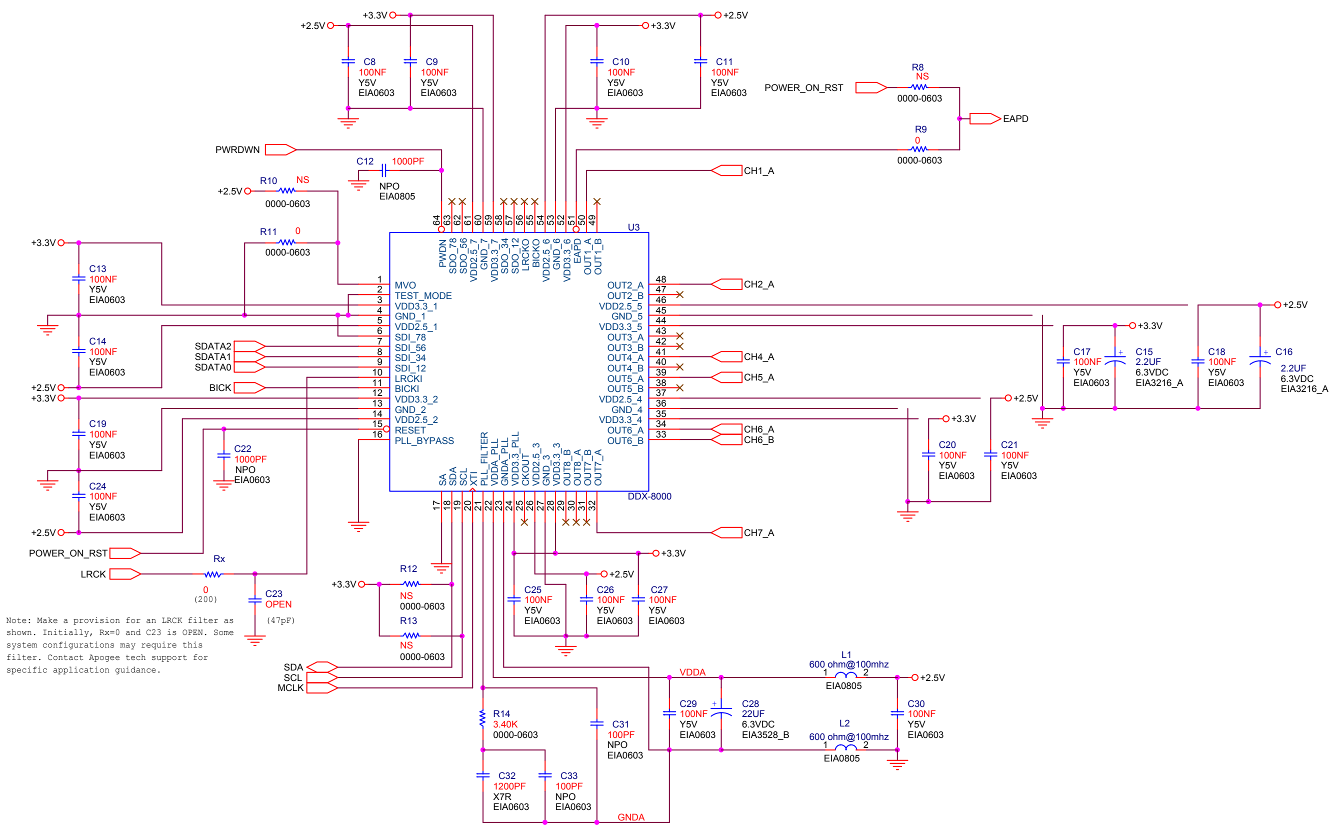

Figure 11. 5.1ch Processing

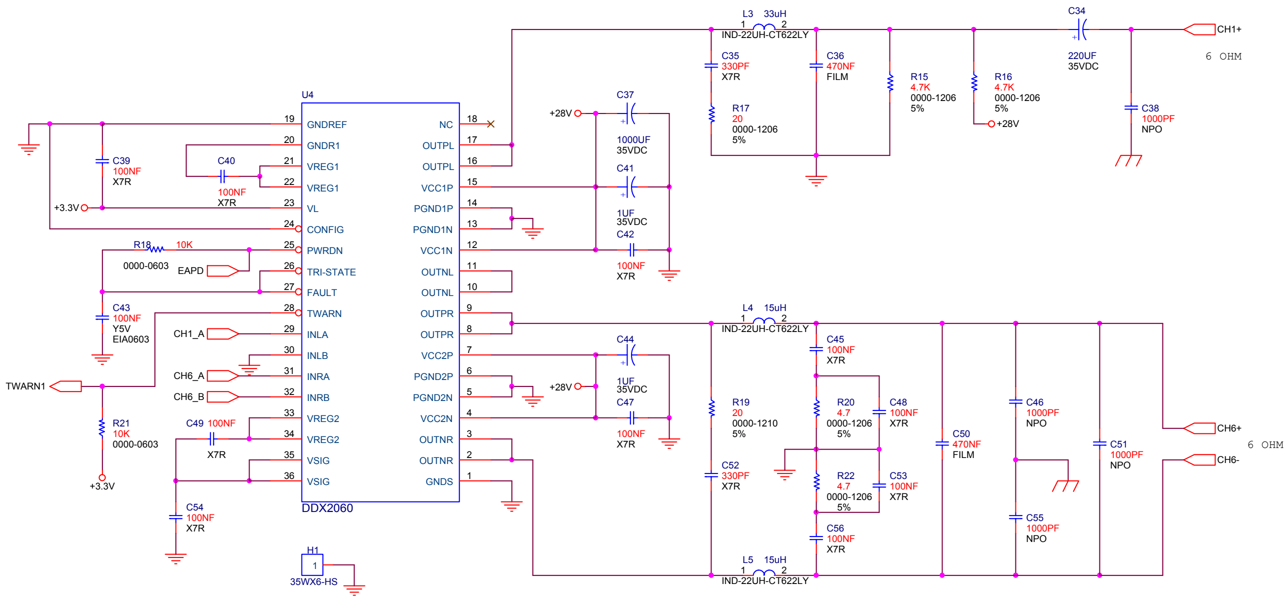

Figure 12. 5.1ch CTR, SUB outputs

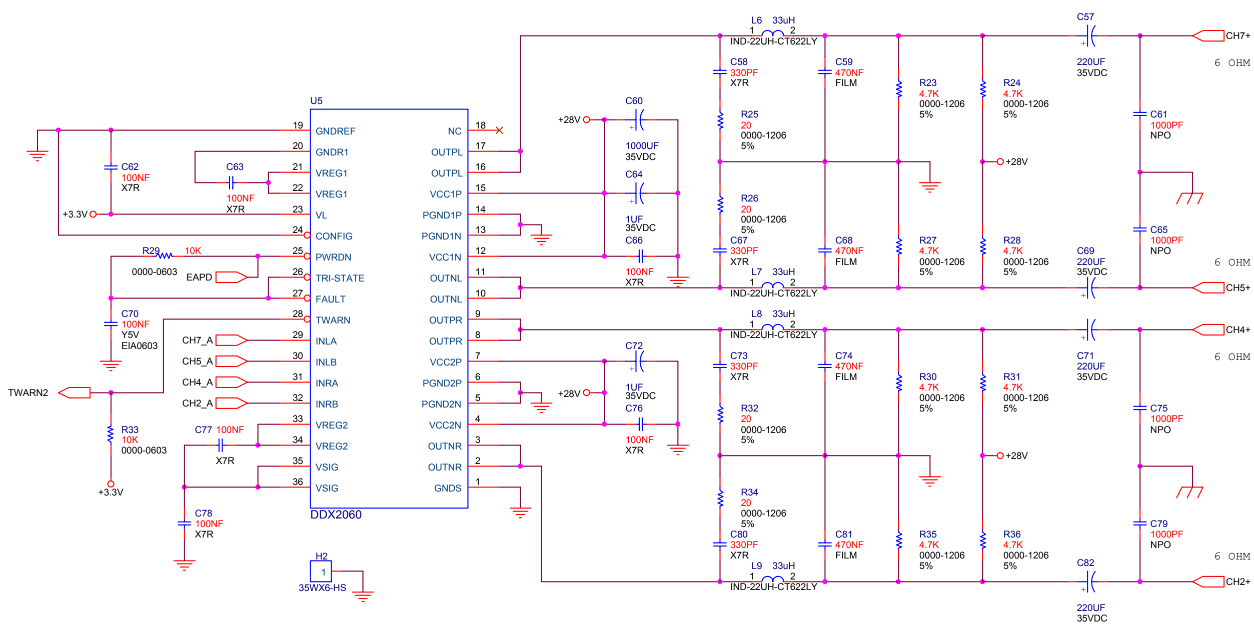

Figure 13. 5.1ch L, R, LS, RS outputs

5.5. 5.1ch Schematic; 2/4/5, 1/3/6 (L/R/SUB, LS/RS/CTR);

This channel mapping locates the L,R and SUB on one power device, LS, RS and CTR on the other. This allows 5.1 or 2.1 channel operation. In 2.1ch operation, the second power device is turned off.

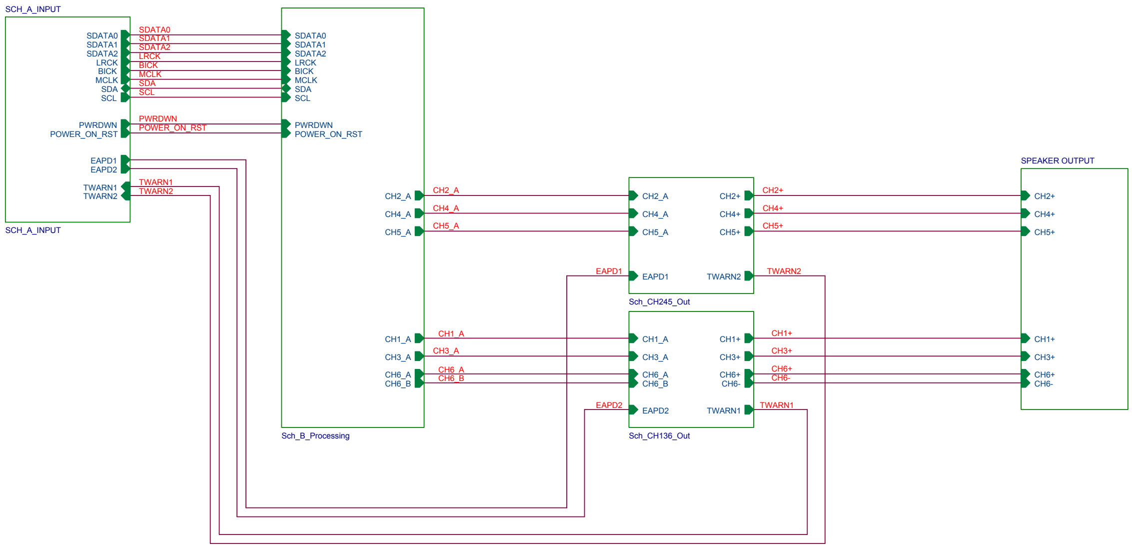

Figure 14. 5.1ch (Alternate) Block Diagram

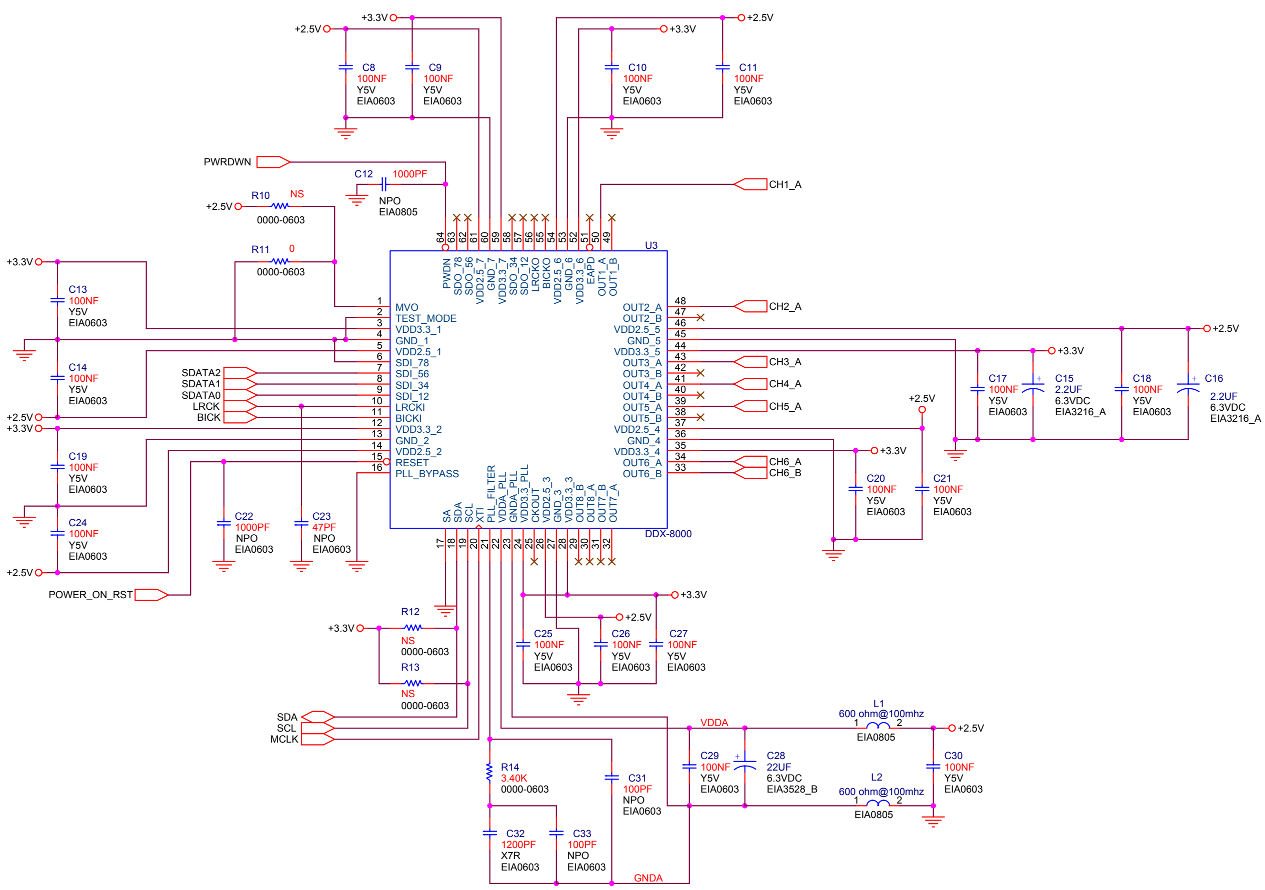

Figure 15. 5.1ch (Alt) Processing

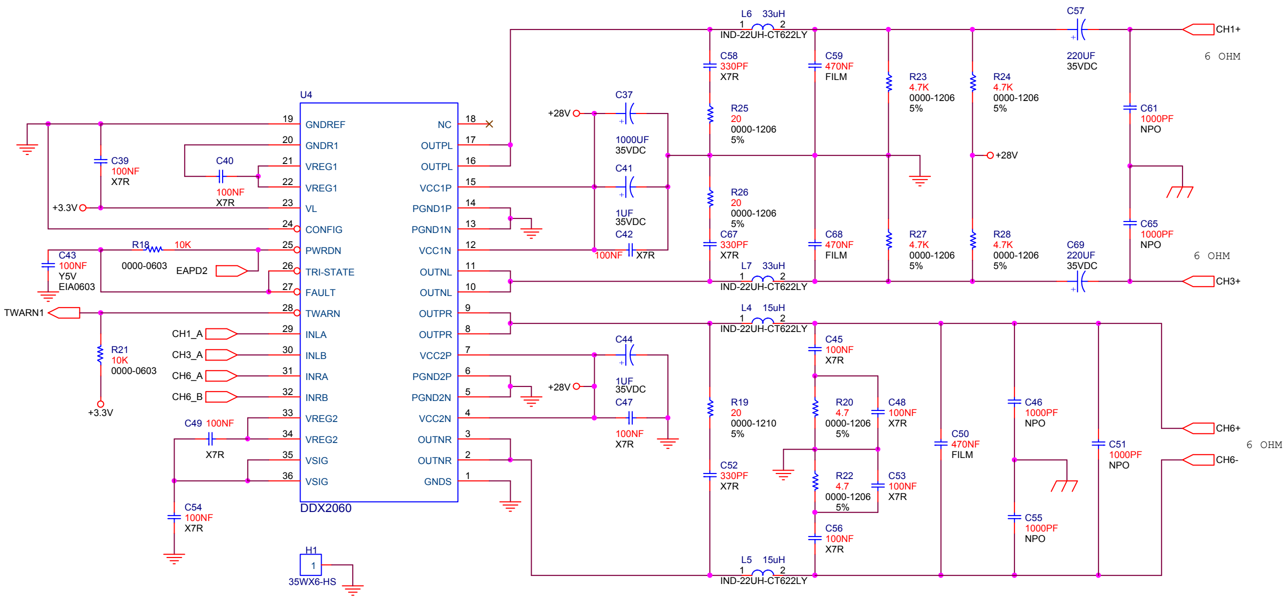

Figure 16. 5.1ch (Alt) L, R, SUB Outputs

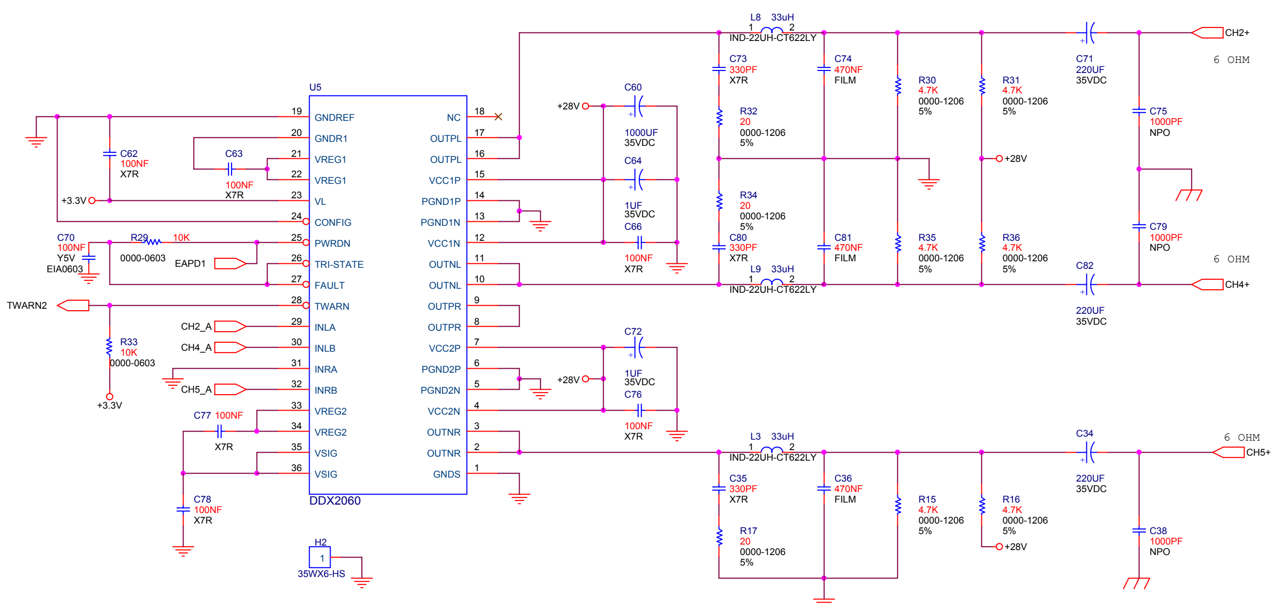

Figure 17. LS, RS, CTR Outputs

5.6. 2.1ch Schematic; 1/3/6 (L, R, SUB)

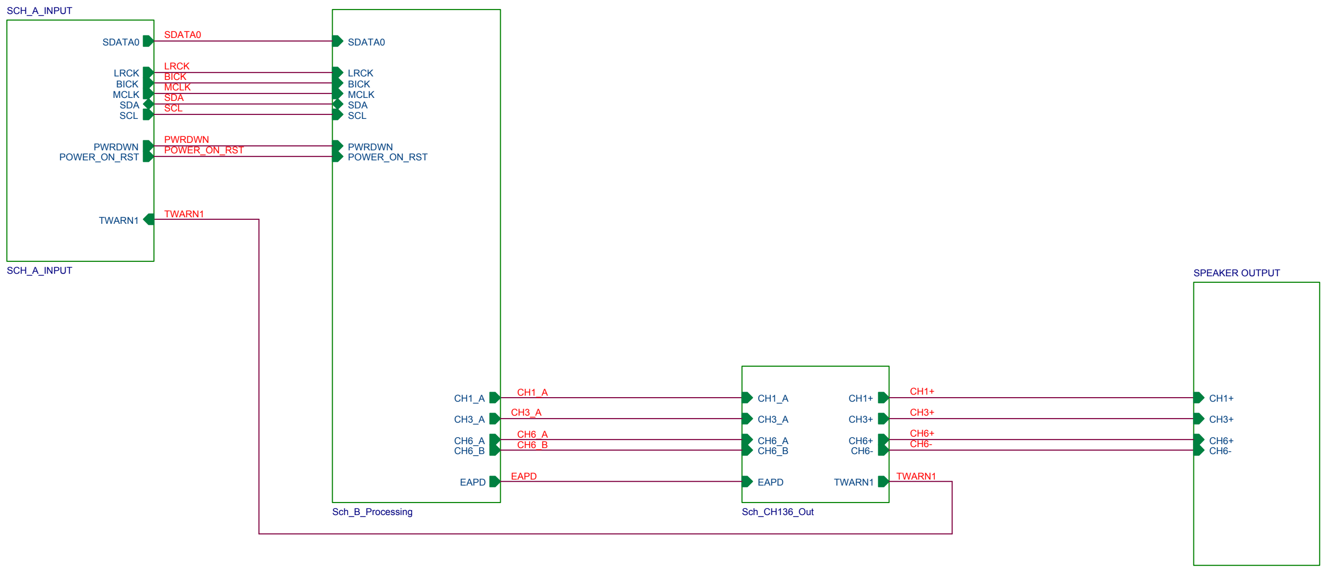

Figure 18. 2.1ch Block Diagram

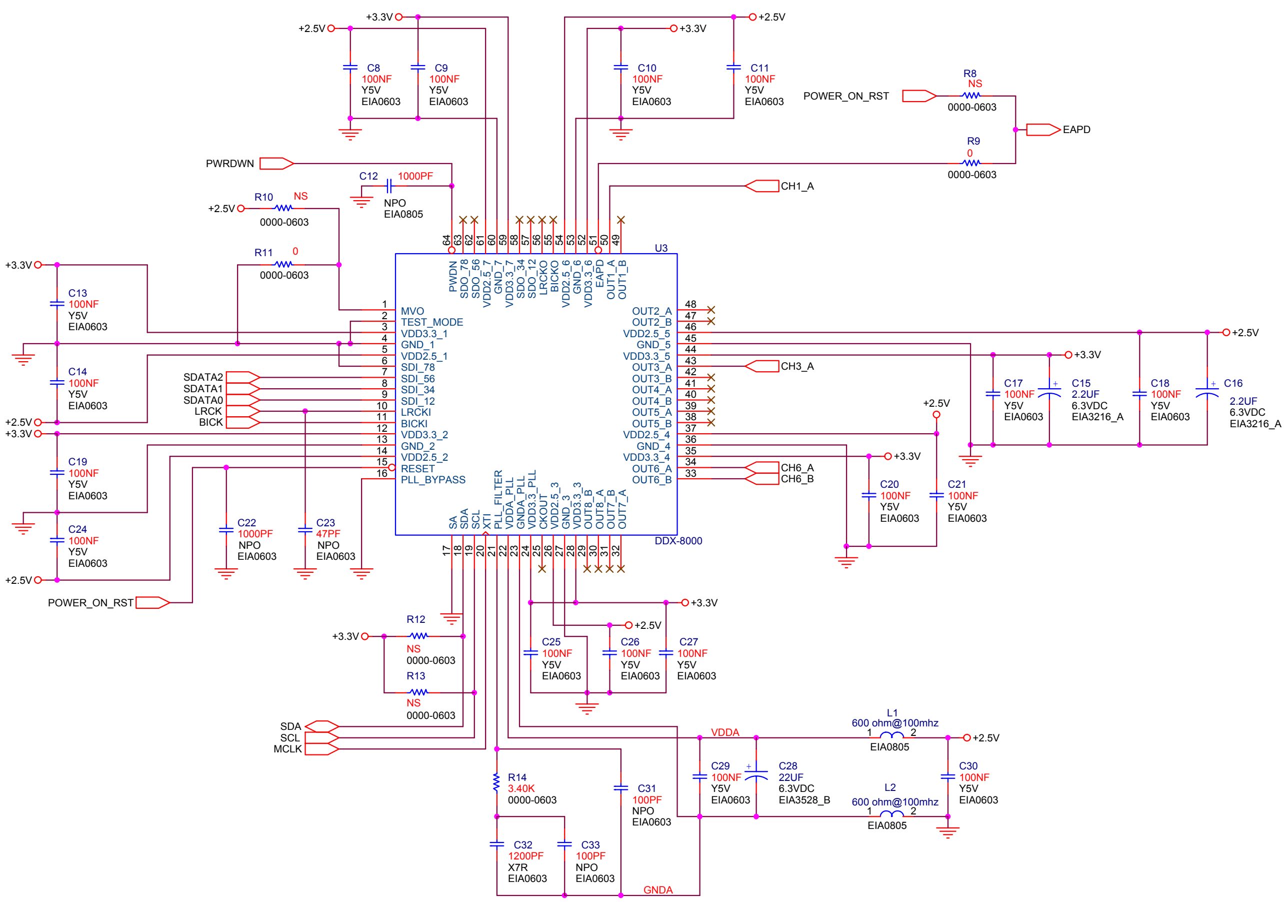

Figure 19. 2.1ch Processing

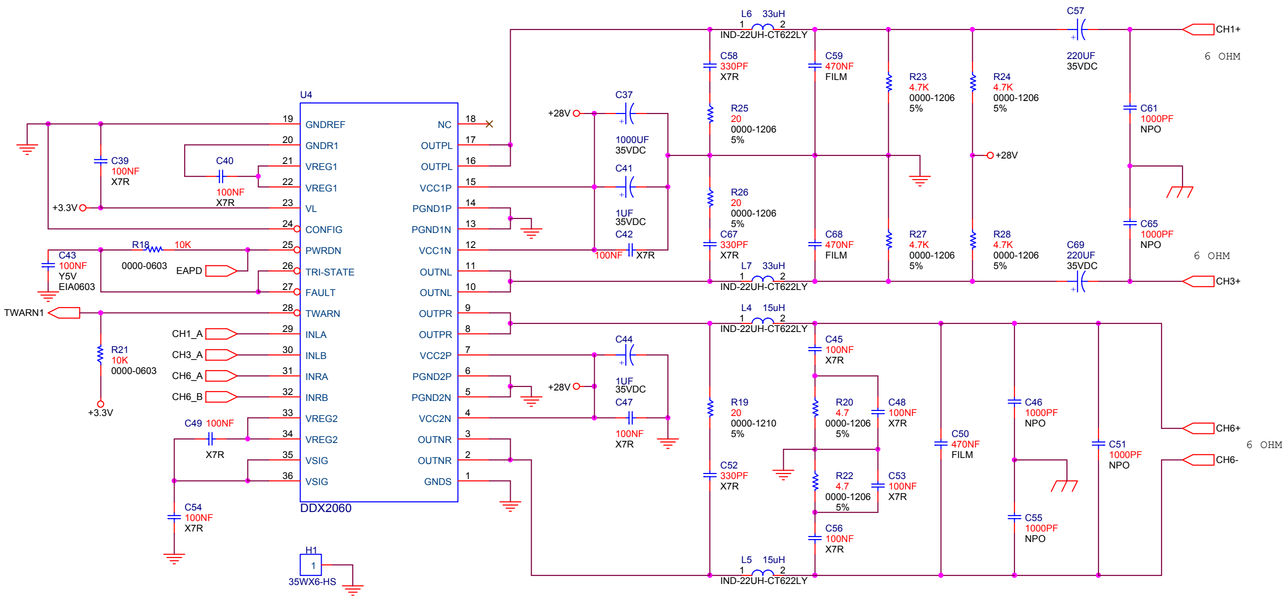

Figure 20. 2.1ch L, R, SUB Outputs